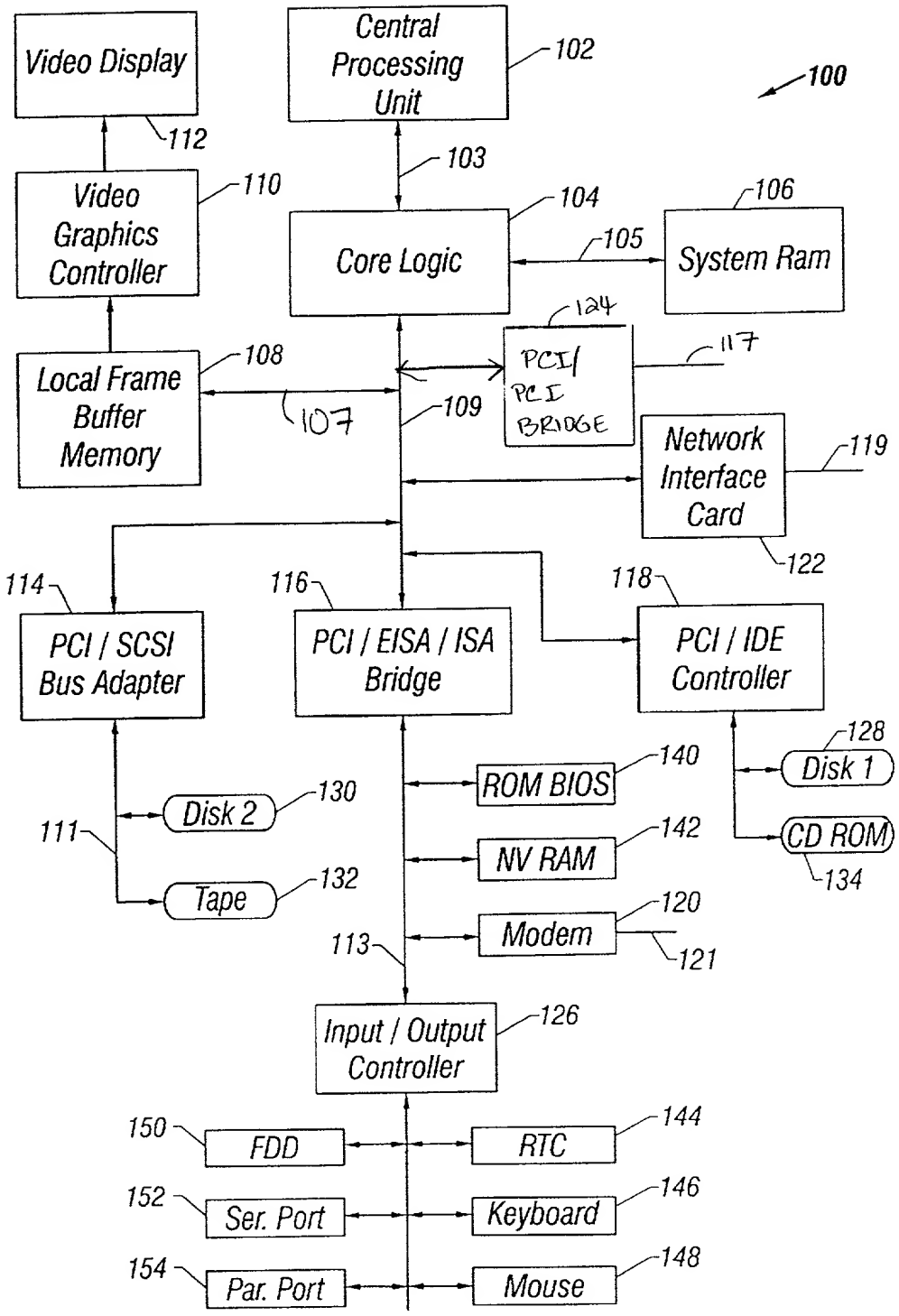
Video Display
112
Central Processing Unit
102
100
103
Video Graphics Controller
110
Core Logic
104
105
System Ram
106
124
PCI/ PCI BRIDGE
117
Local Frame Buffer Memory
108
107
109
Network Interface Card
119
122
114
116
118
PCI / SCSI Bus Adapter
PCI / EISA / ISA Bridge
PCI / IDE Controller
128
Disk 1
CD ROM
134
ROM BIOS
140
NV RAM
142
Modem
120
121
Disk 2
130
111
Tape
132
113
Input / Output Controller
126
150
FDD
RTC
144
152
Ser. Port
Keyboard
146
154
Par. Port
Mouse
148

FIG. 1

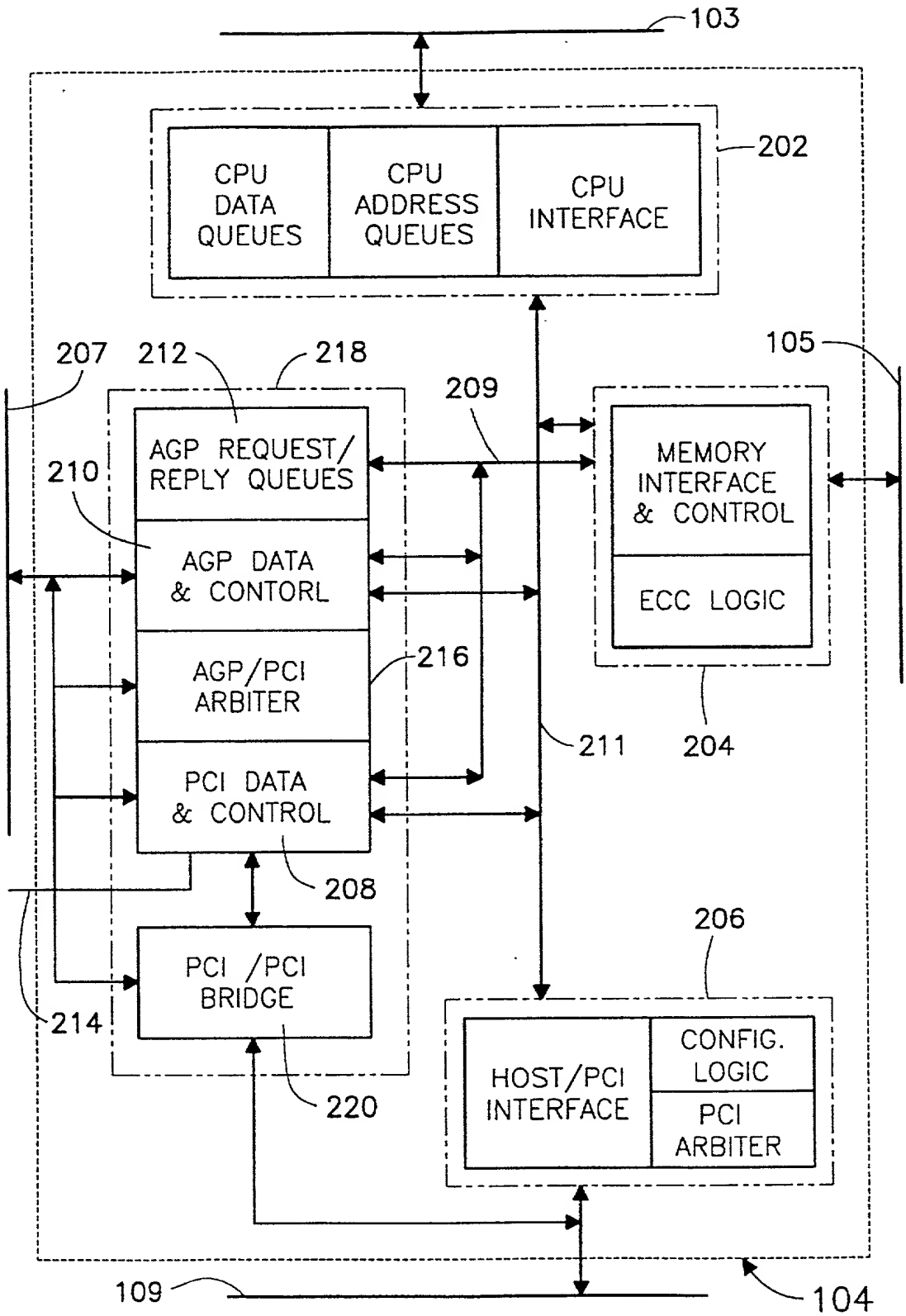
103
CPU DATA QUEUES
CPU ADDRESS QUEUES
CPU INTERFACE
202
207
212
218
209
105
AGP REQUEST/ REPLY QUEUES
210
AGP DATA & CONTORL
AGP/PCI ARBITER
216
PCI DATA & CONTROL
208
MEMORY INTERFACE & CONTROL
ECC LOGIC
211
204
206
PCI /PCI BRIDGE
214
220
HOST/PCI INTERFACE
CONFIG. LOGIC
PCI ARBITER
109
104

FIGURE 2

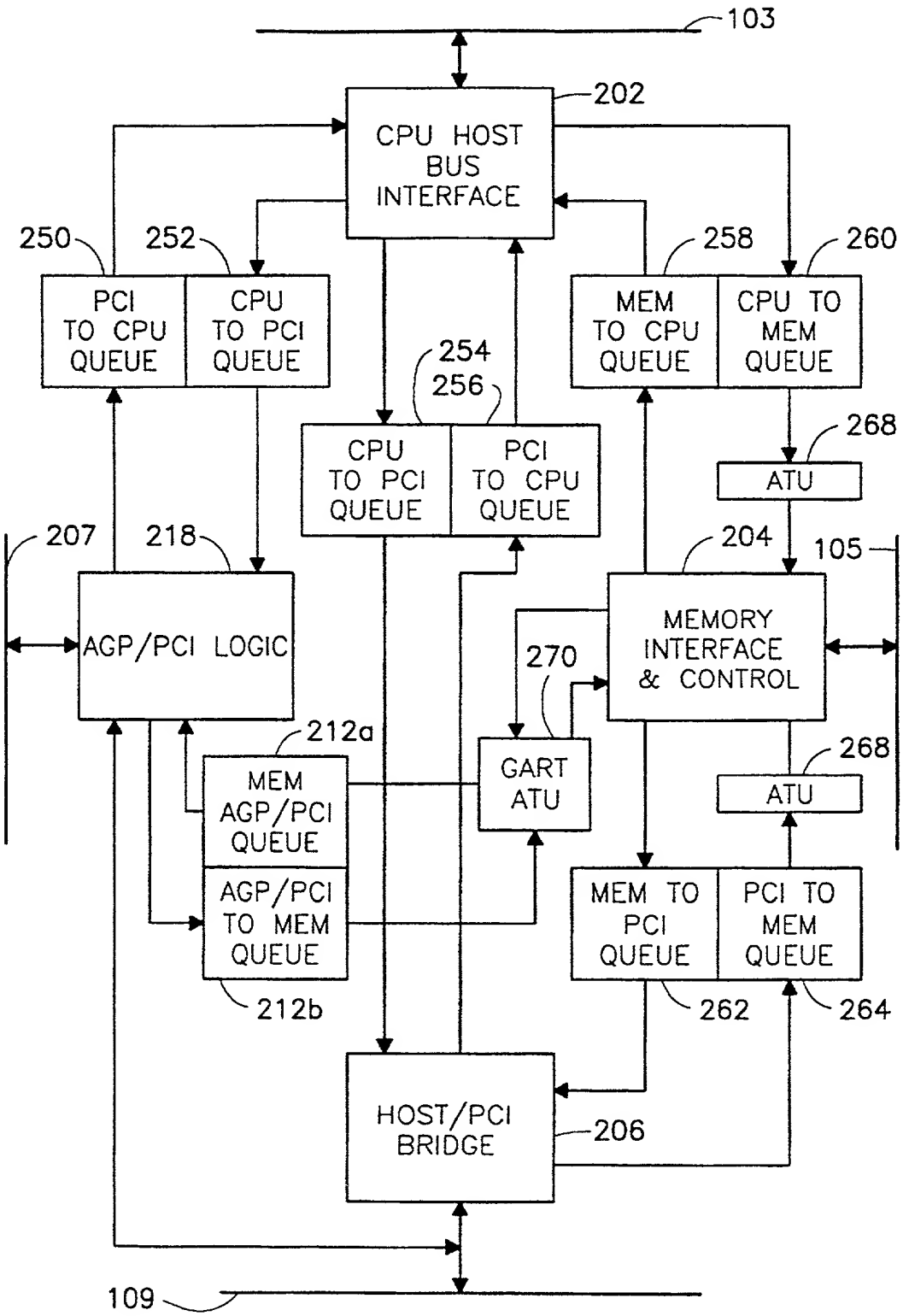
103
202
CPU HOST BUS INTERFACE
250
252
PCI TO CPU QUEUE
CPU TO PCI QUEUE
254
256
CPU TO PCI QUEUE
PCI TO CPU QUEUE
258
260
MEM TO CPU QUEUE
CPU TO MEM QUEUE
268
ATU
207
218
AGP/PCI LOGIC
204
105
MEMORY INTERFACE & CONTROL
270
212a
MEM AGP/PCI QUEUE
AGP/PCI TO MEM QUEUE
212b
GART ATU
268
ATU
MEM TO PCI QUEUE
PCI TO MEM QUEUE
262
264
HOST/PCI BRIDGE
206
109

FIGURE 2A

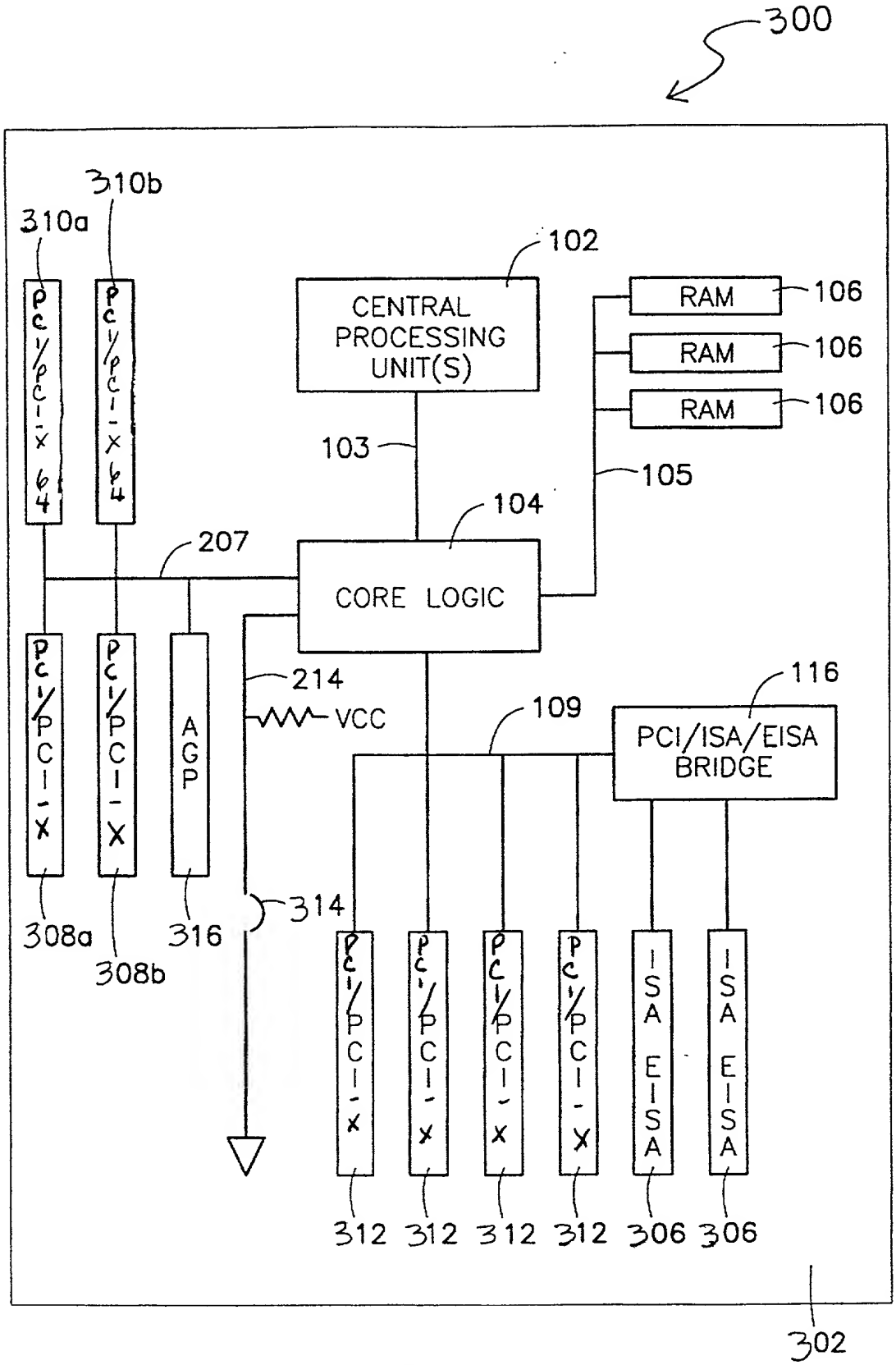
300
310b
310a
102
CENTRAL PROCESSING UNIT(S)
RAM
106
RAM
106
RAM
106
103
105
104
207
CORE LOGIC
214
VCC
116
109
PCI/ISA/EISA BRIDGE
AGP
314
308a
308b
316
312
312
312
312
306
306
302

FIGURE 3

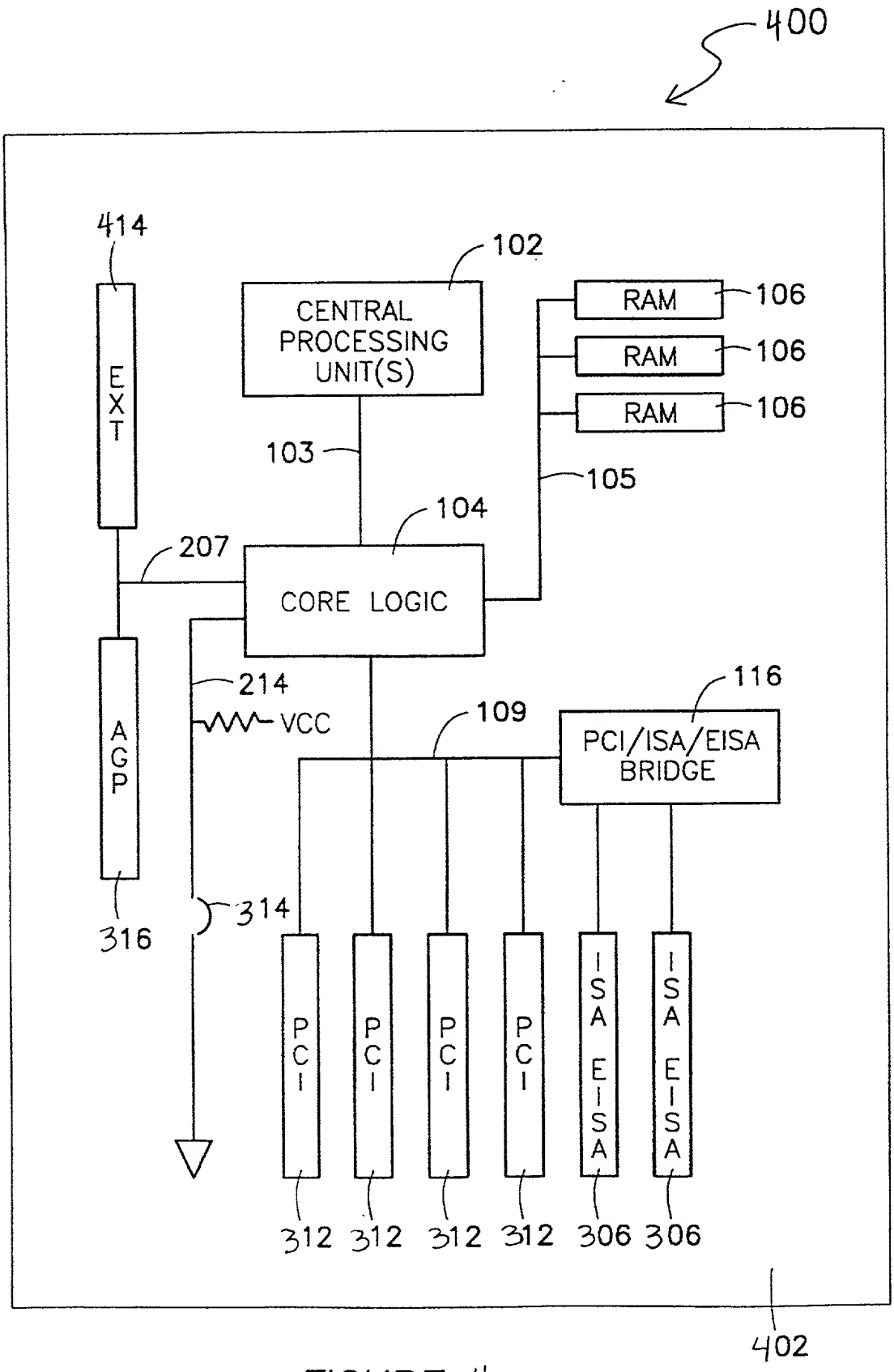
400
414
102
CENTRAL PROCESSING UNIT(S)
RAM
106
RAM
106
RAM
106
EXT
103
105
104
207
CORE LOGIC
214
VCC
116
109
PCI/ISA/EISA BRIDGE
AGP
316
314
PCI
PCI
PCI
PCI
ISA EISA
ISA EISA
312
312
312
312
306
306
402

FIGURE 4

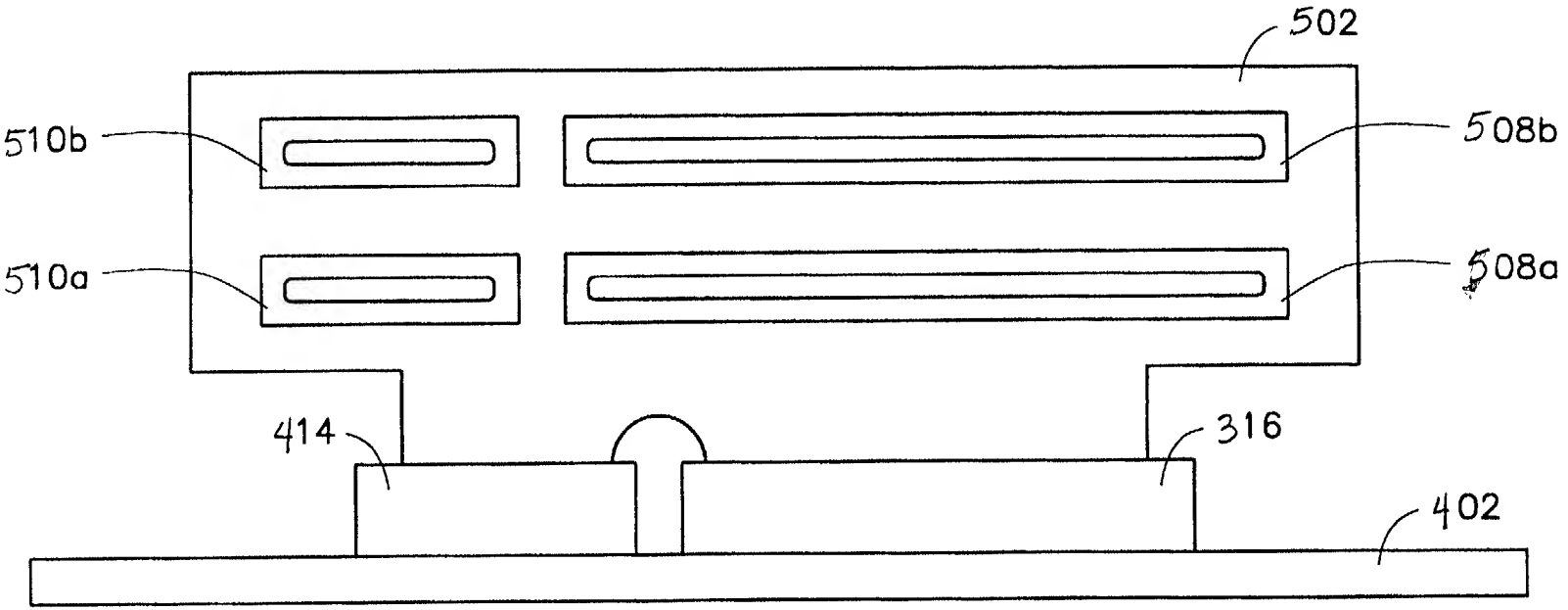

FIGURE 5

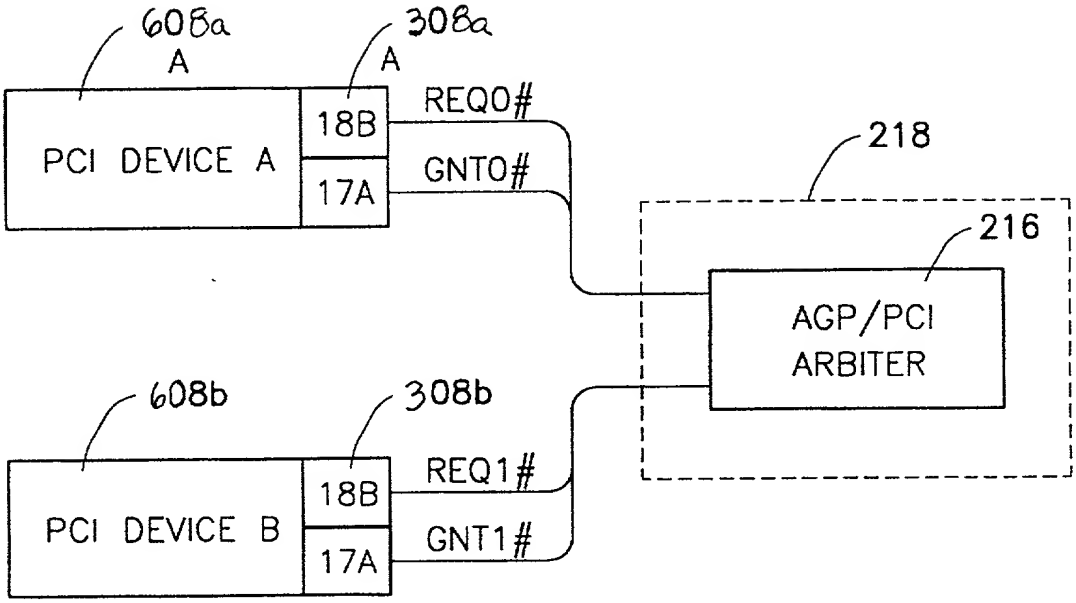

FIGURE 6

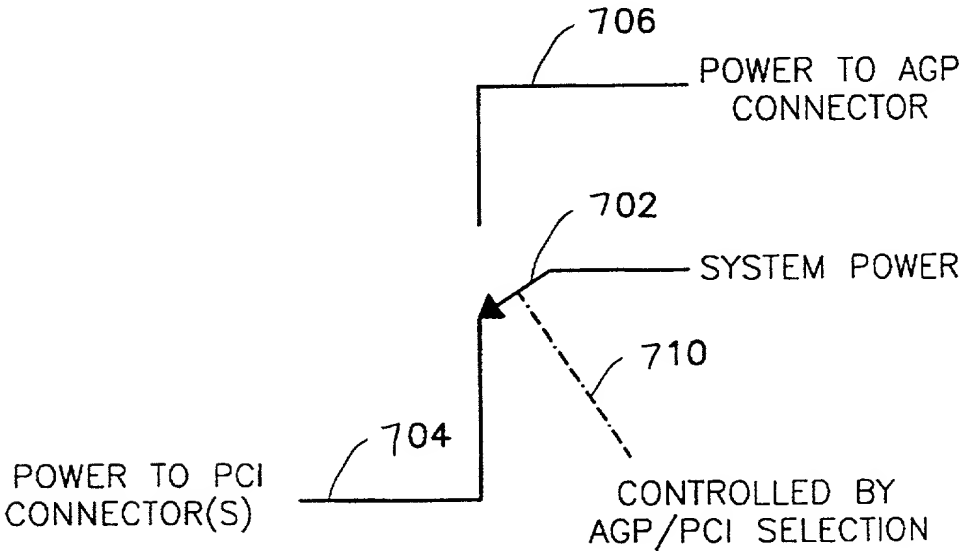

FIGURE 7

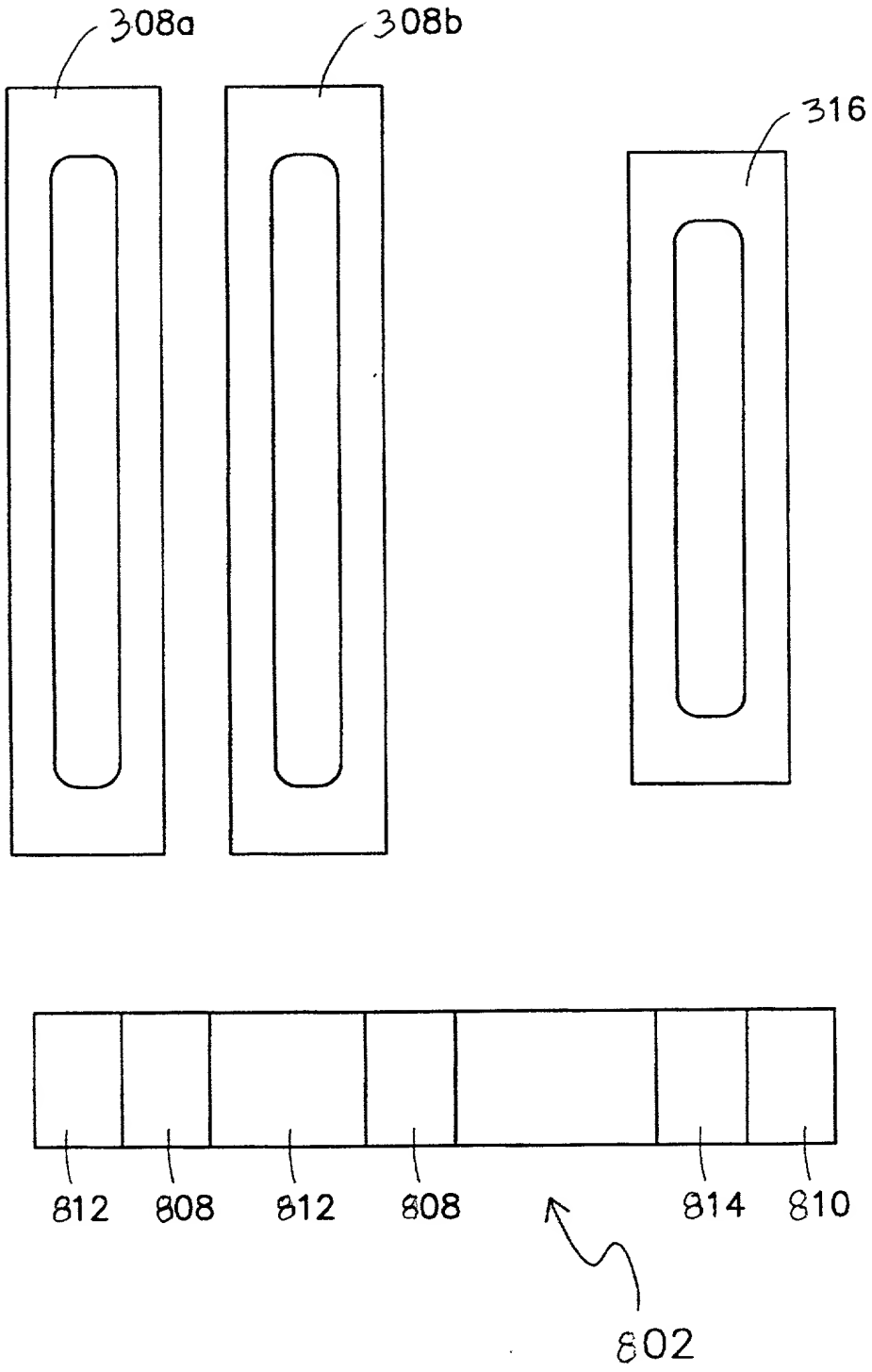

FIGURE 8A

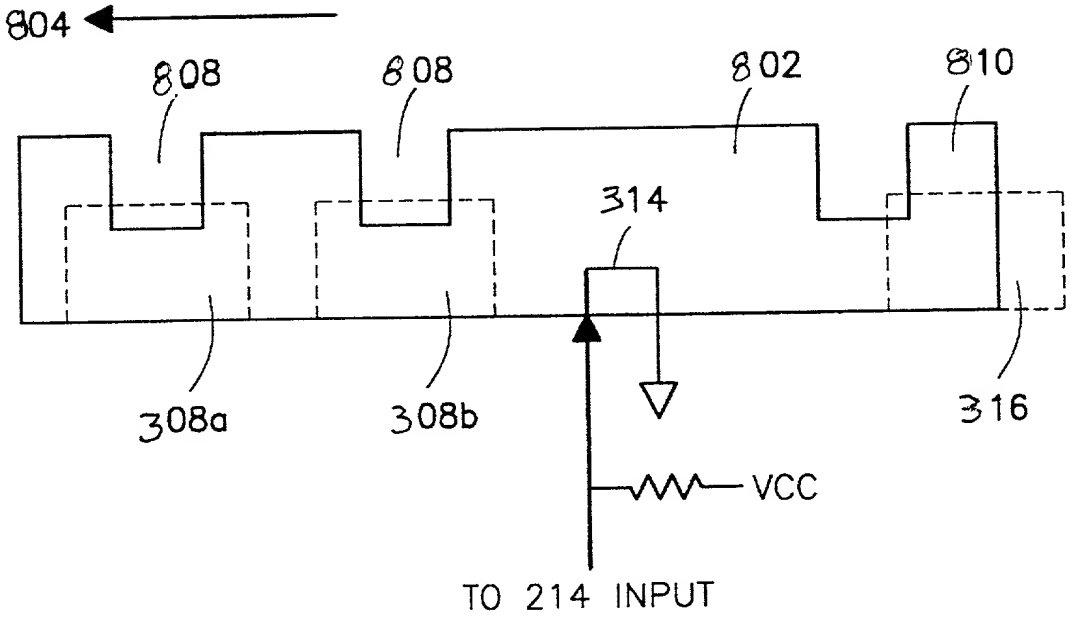

FIGURE 8B

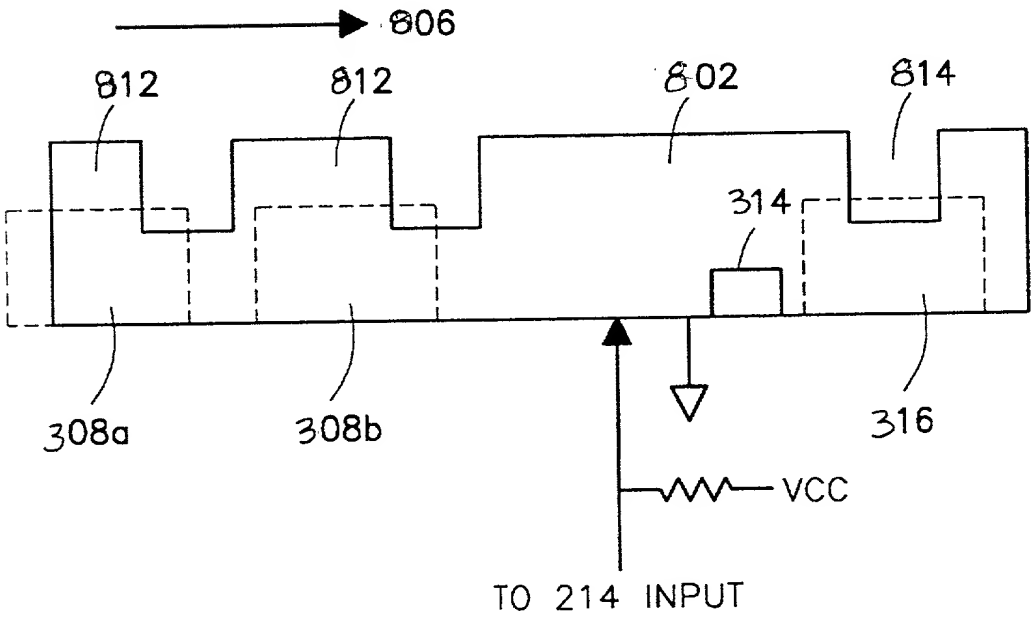

FIGURE 8C

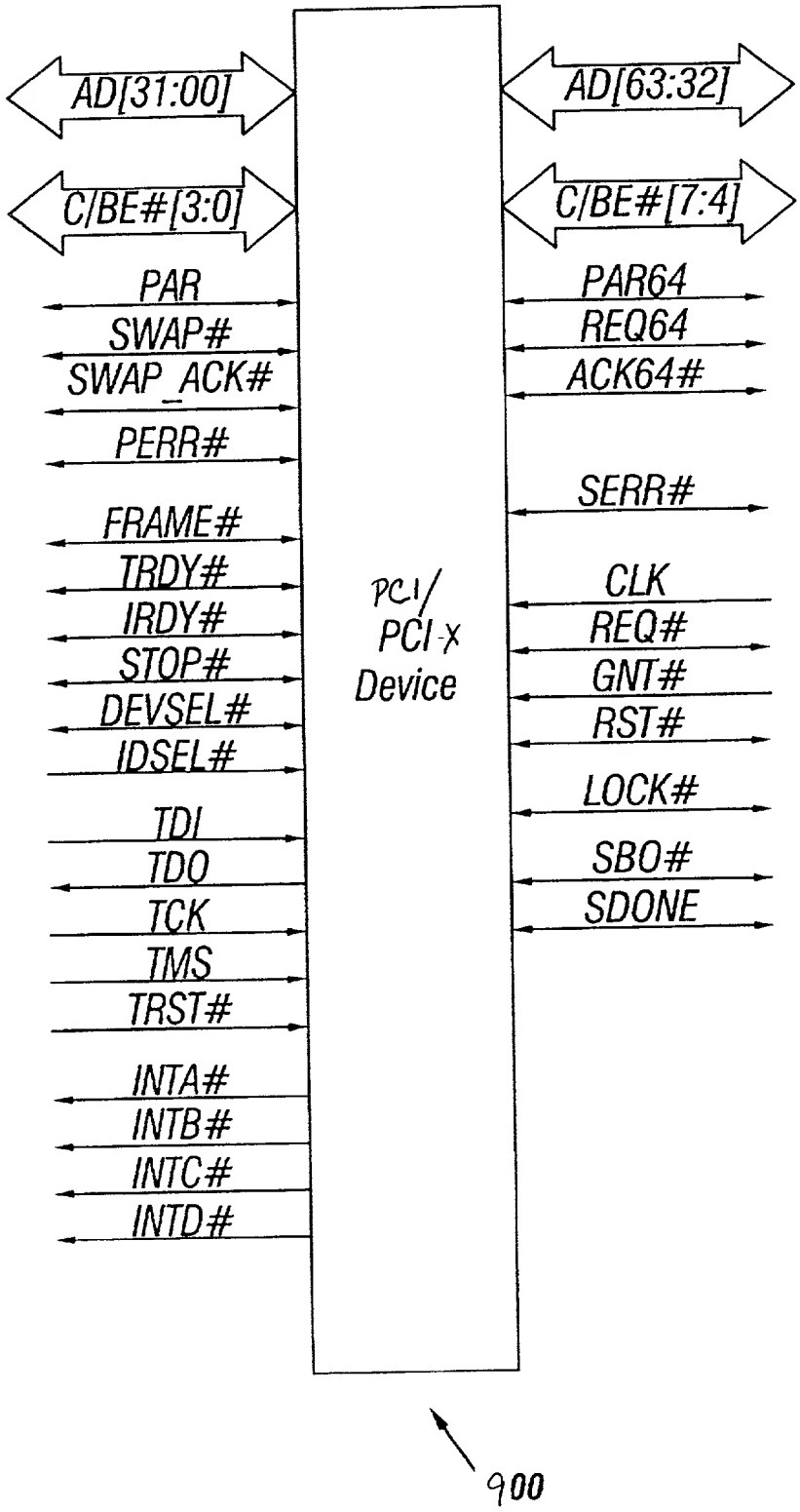
AD[31:00]
AD[63:32]
C/BE#[3:0]
C/BE#[7:4]
PAR
SWAP#
SWAP_ACK#
PERR#
FRAME#
TRDY#
IRDY#
STOP#
DEVSEL#
IDSEL#
TDI
TDO
TCK
TMS
TRST#
INTA#
INTB#
INTC#
INTD#
PCI/
PCI-X
Device
PAR64
REQ64
ACK64#
SERR#
CLK
REQ#
GNT#
RST#
LOCK#
SBO#
SDONE
900

FIG. 9

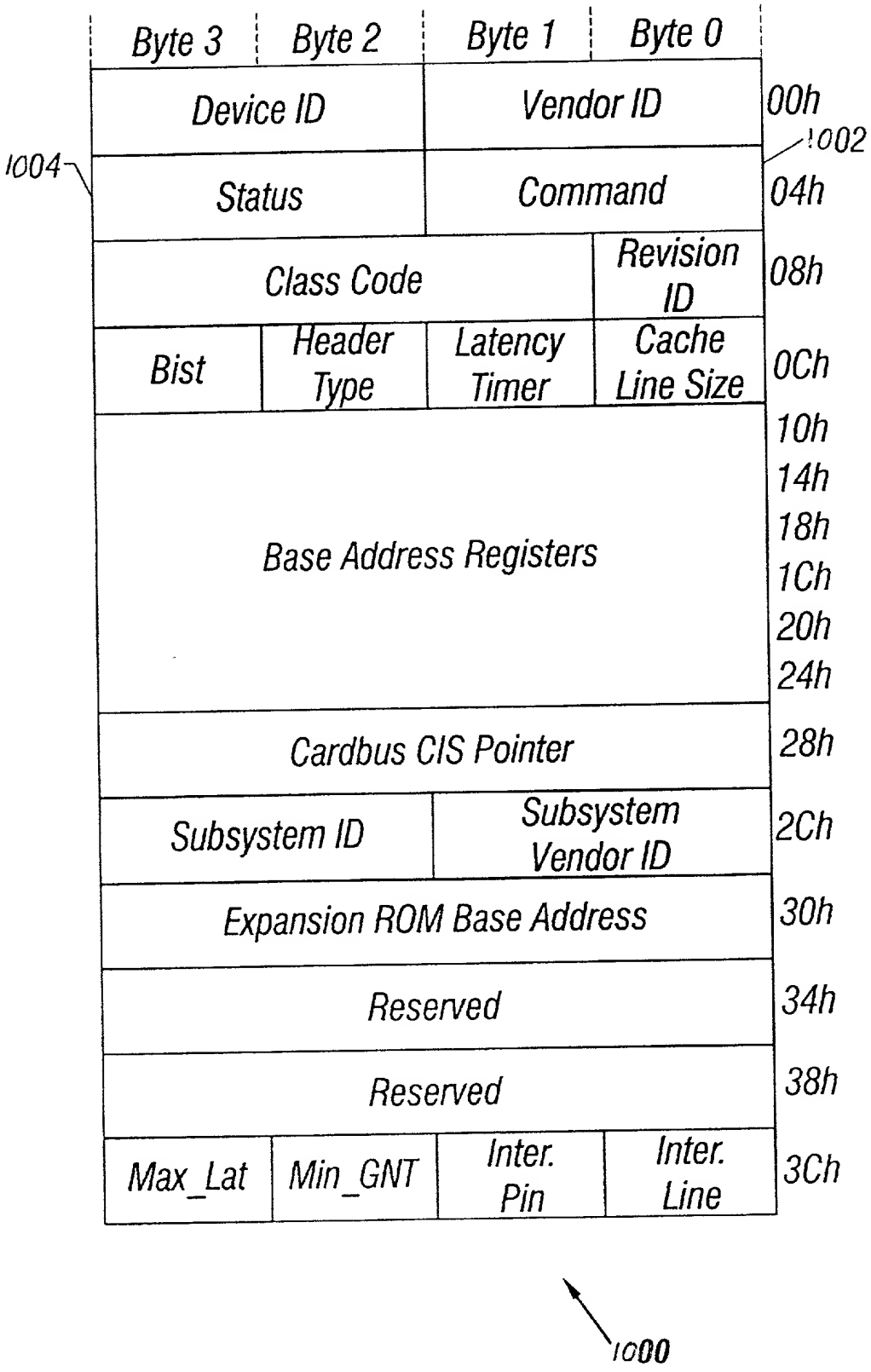
Byte 3
Byte 2
Byte 1
Byte 0
Device ID
Vendor ID
00h
1002
1004
Status
Command
04h
Class Code
Revision ID
08h
Bist
Header Type
Latency Timer
Cache Line Size
0Ch
10h
14h
18h
1Ch
20h
24h
Base Address Registers
Cardbus CIS Pointer
28h
Subsystem ID
Subsystem Vendor ID
2Ch
Expansion ROM Base Address
30h
Reserved
34h
Reserved
38h
Max_Lat
Min_GNT
Inter. Pin
Inter. Line
3Ch
1000

FIG. 10

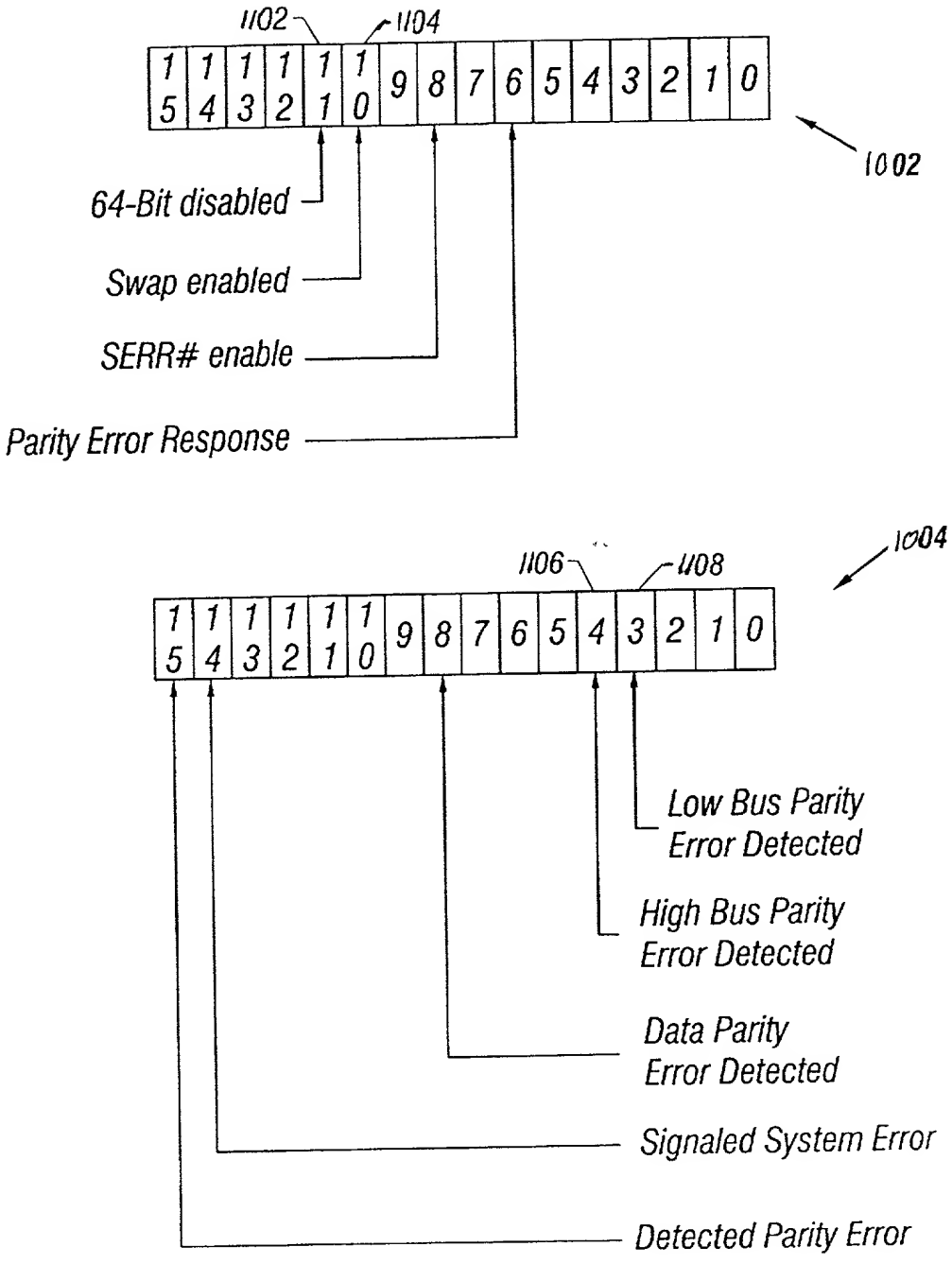
1102
1104
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1002
64-Bit disabled
Swap enabled
SERR# enable
Parity Error Response
1004
1106
1108
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Low Bus Parity Error Detected
High Bus Parity Error Detected
Data Parity Error Detected
Signaled System Error
Detected Parity Error

FIG. 11

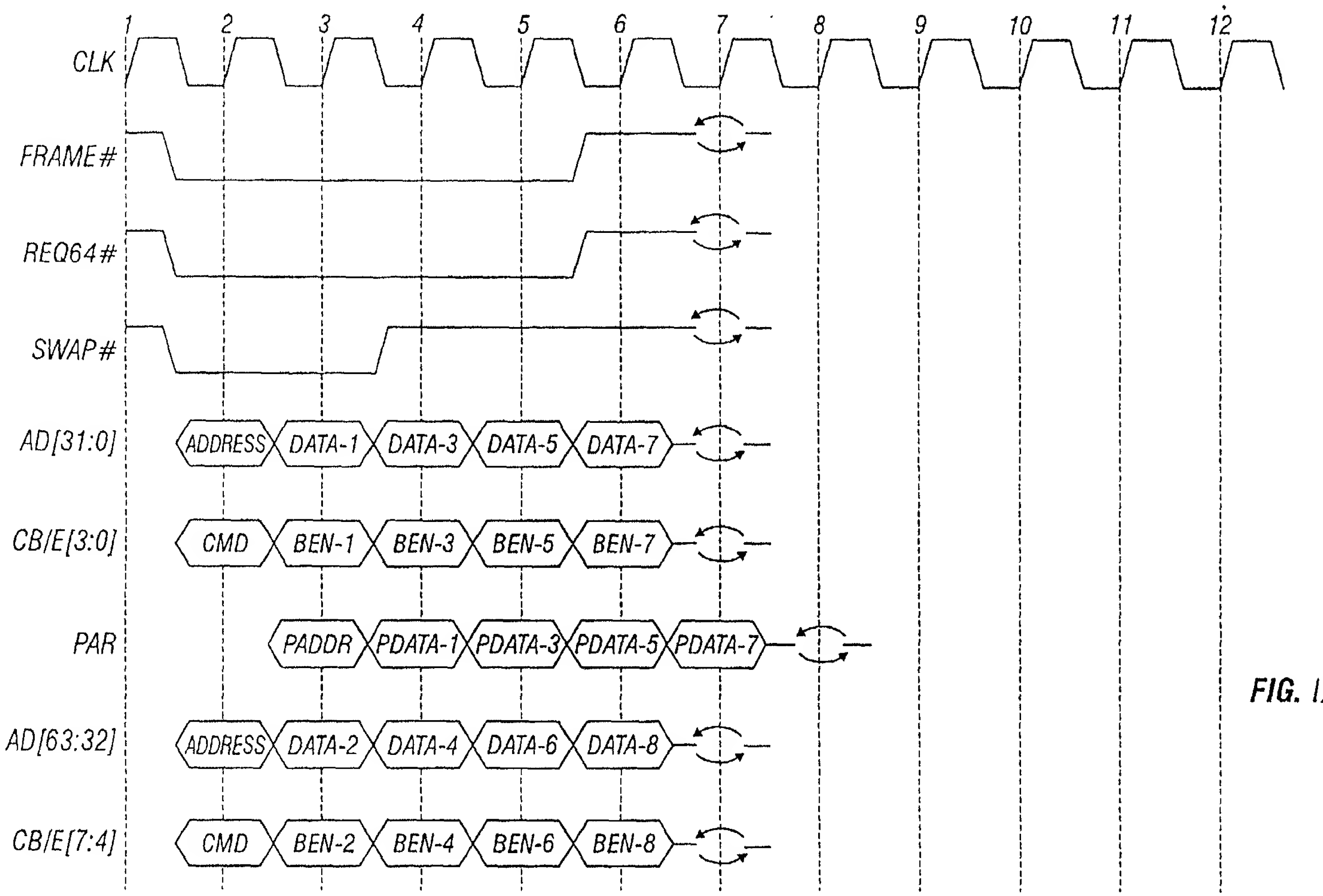
1
2
3
4
5
6
7
8
9
10
11
12
CLK
FRAME#
REQ64#
SWAP#
AD[31:0]
ADDRESS
DATA-1
DATA-3
DATA-5
DATA-7
CB/E[3:0]
CMD
BEN-1
BEN-3
BEN-5
BEN-7
PAR
PADDR
PDATA-1
PDATA-3
PDATA-5
PDATA-7
AD[63:32]
ADDRESS
DATA-2
DATA-4
DATA-6
DATA-8
CB/E[7:4]
CMD
BEN-2
BEN-4
BEN-6
BEN-8

FIG. 12A

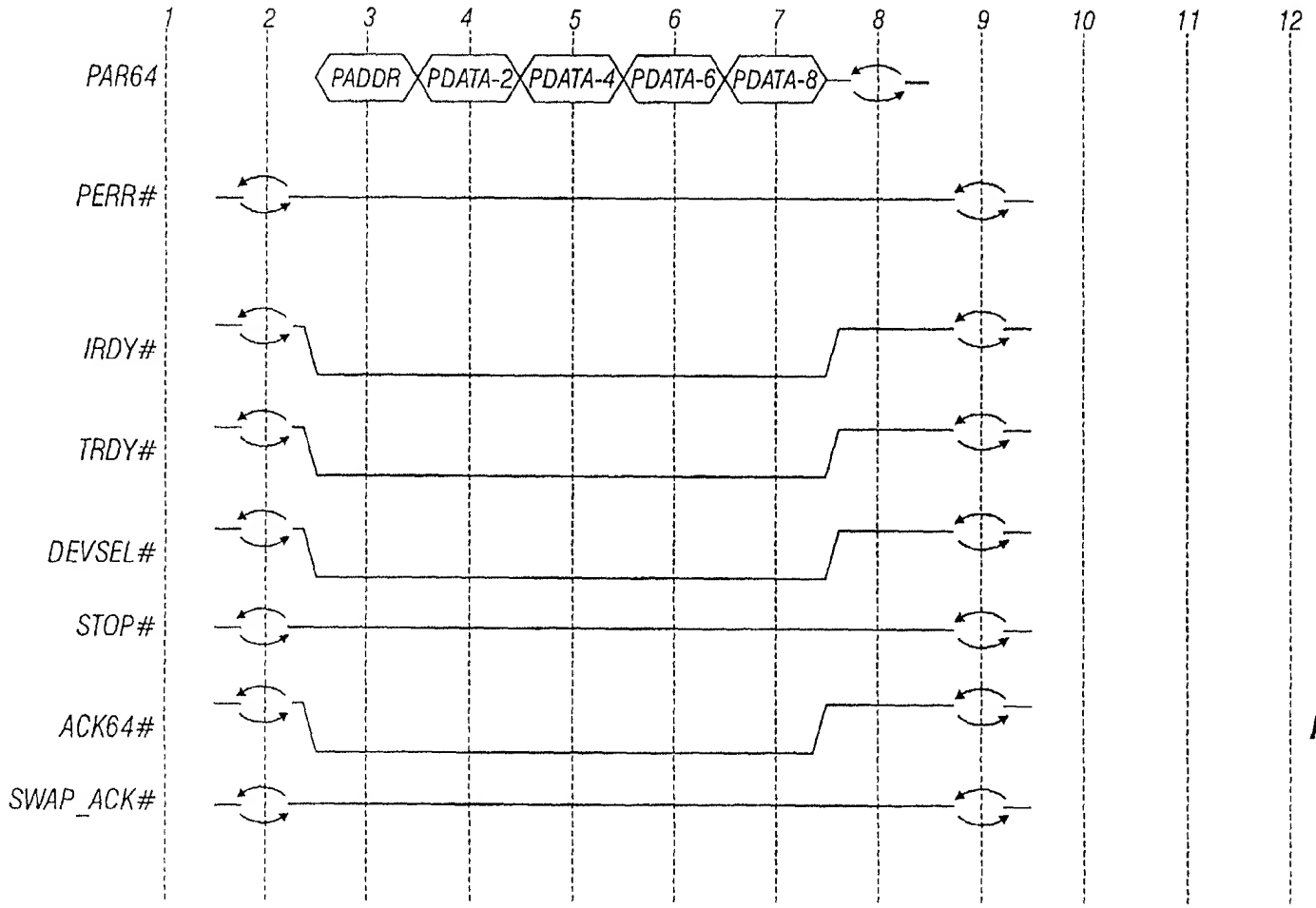
1
2
3
4
5
6
7
8
9
10
11
12
PAR64
PADDR
PDATA-2
PDATA-4
PDATA-6
PDATA-8
PERR#
IRDY#
TRDY#
DEVSEL#
STOP#
ACK64#
SWAP_ACK#

FIG. 12B

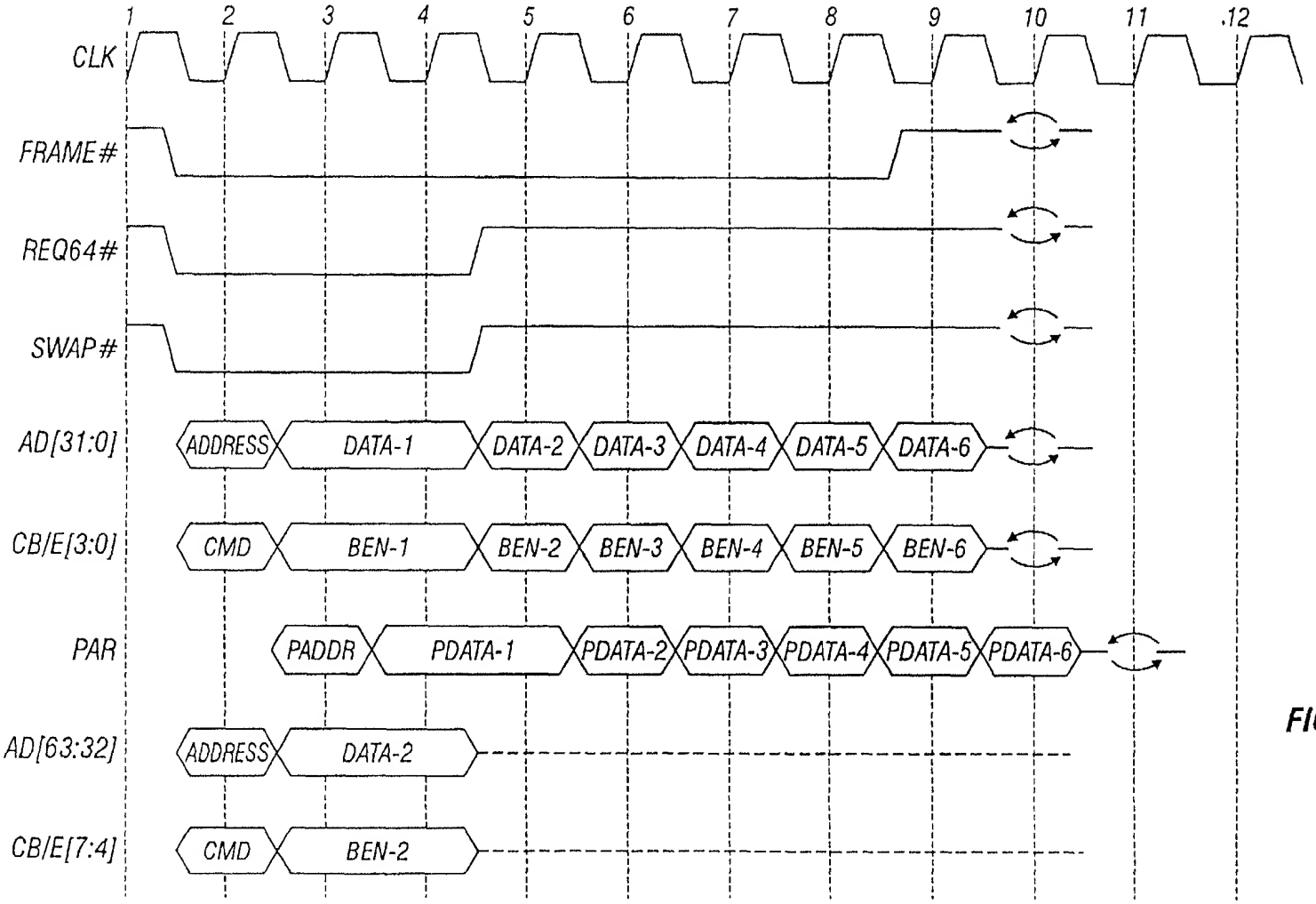
1
2
3
4
5
6
7
8
9
10
11
12
CLK
FRAME#
REQ64#
SWAP#
AD[31:0]
ADDRESS
DATA-1
DATA-2
DATA-3
DATA-4
DATA-5
DATA-6
CB/E[3:0]
CMD
BEN-1
BEN-2
BEN-3
BEN-4
BEN-5
BEN-6
PAR
PADDR
PDATA-1
PDATA-2
PDATA-3
PDATA-4
PDATA-5
PDATA-6
AD[63:32]
ADDRESS
DATA-2
CB/E[7:4]
CMD
BEN-2

FIG. 13A

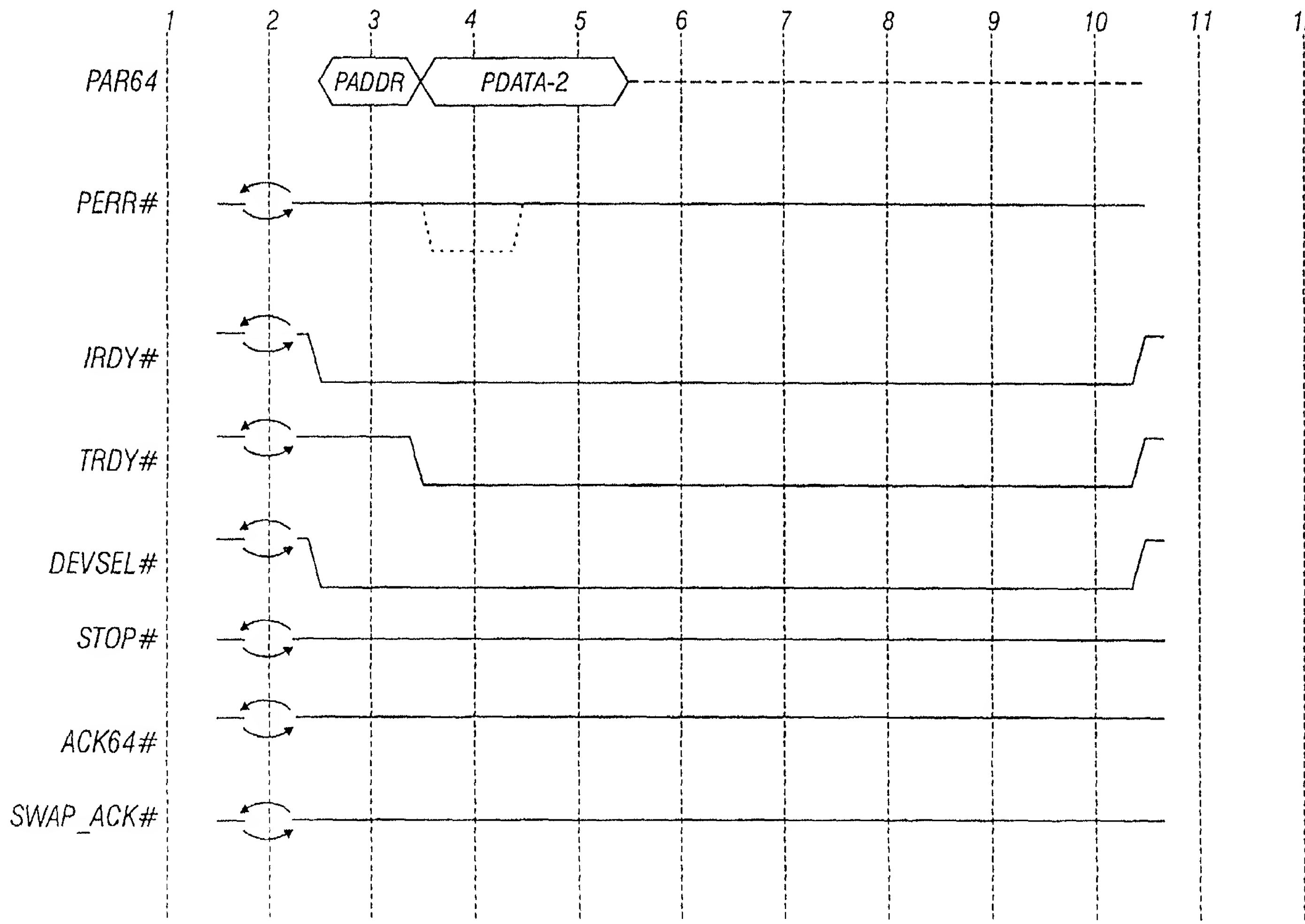
1
2
3
4
5
6
7
8
9
10
11
12
PAR64
PADDR
PDATA-2
PERR#
IRDY#
TRDY#
DEVSEL#
STOP#
ACK64#
SWAP_ACK#

FIG. 13B

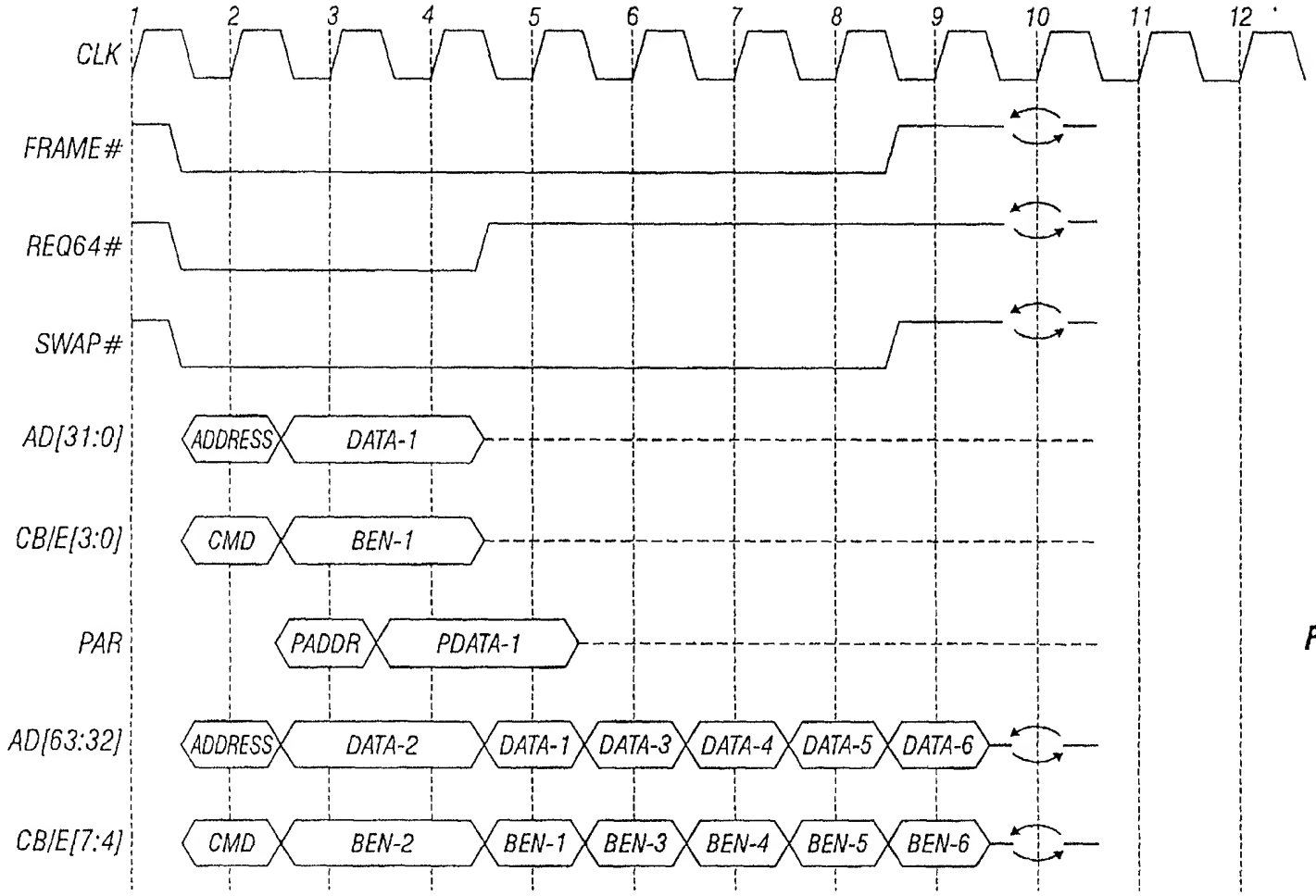
1
2
3
4
5
6
7
8
9
10
11
12
CLK
FRAME#
REQ64#
SWAP#
AD[31:0]
ADDRESS
DATA-1
CB/E[3:0]
CMD
BEN-1
PAR
PADDR
PDATA-1
AD[63:32]
ADDRESS
DATA-2
DATA-1
DATA-3
DATA-4
DATA-5
DATA-6
CB/E[7:4]
CMD
BEN-2
BEN-1
BEN-3
BEN-4
BEN-5
BEN-6

FIG. 14A

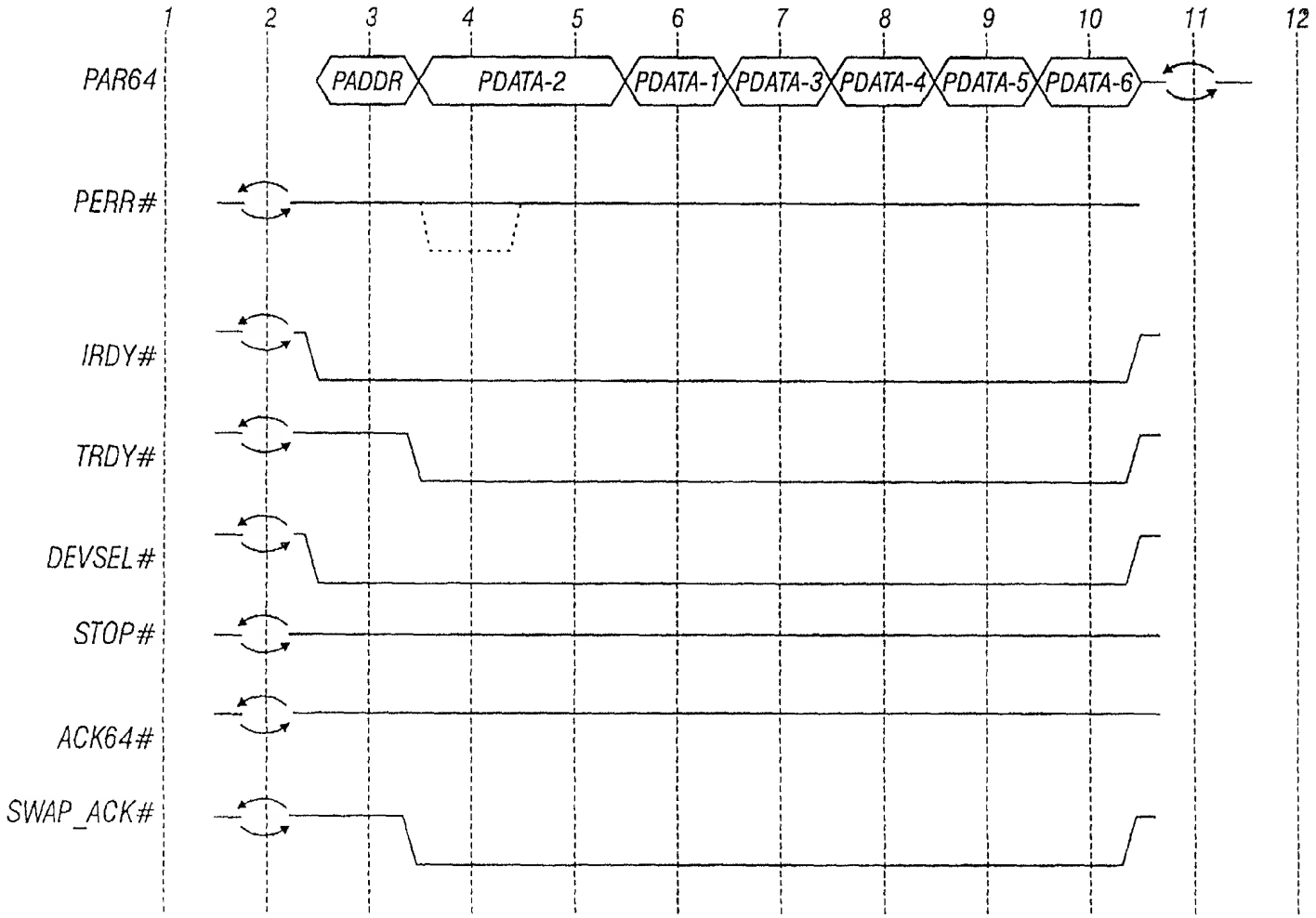
1
2
3
4
5
6
7
8
9
10
11
12
PAR64
PADDR
PDATA-2
PDATA-1
PDATA-3
PDATA-4
PDATA-5
PDATA-6
PERR#
IRDY#
TRDY#
DEVSEL#
STOP#
ACK64#
SWAP_ACK#

FIG. 14B

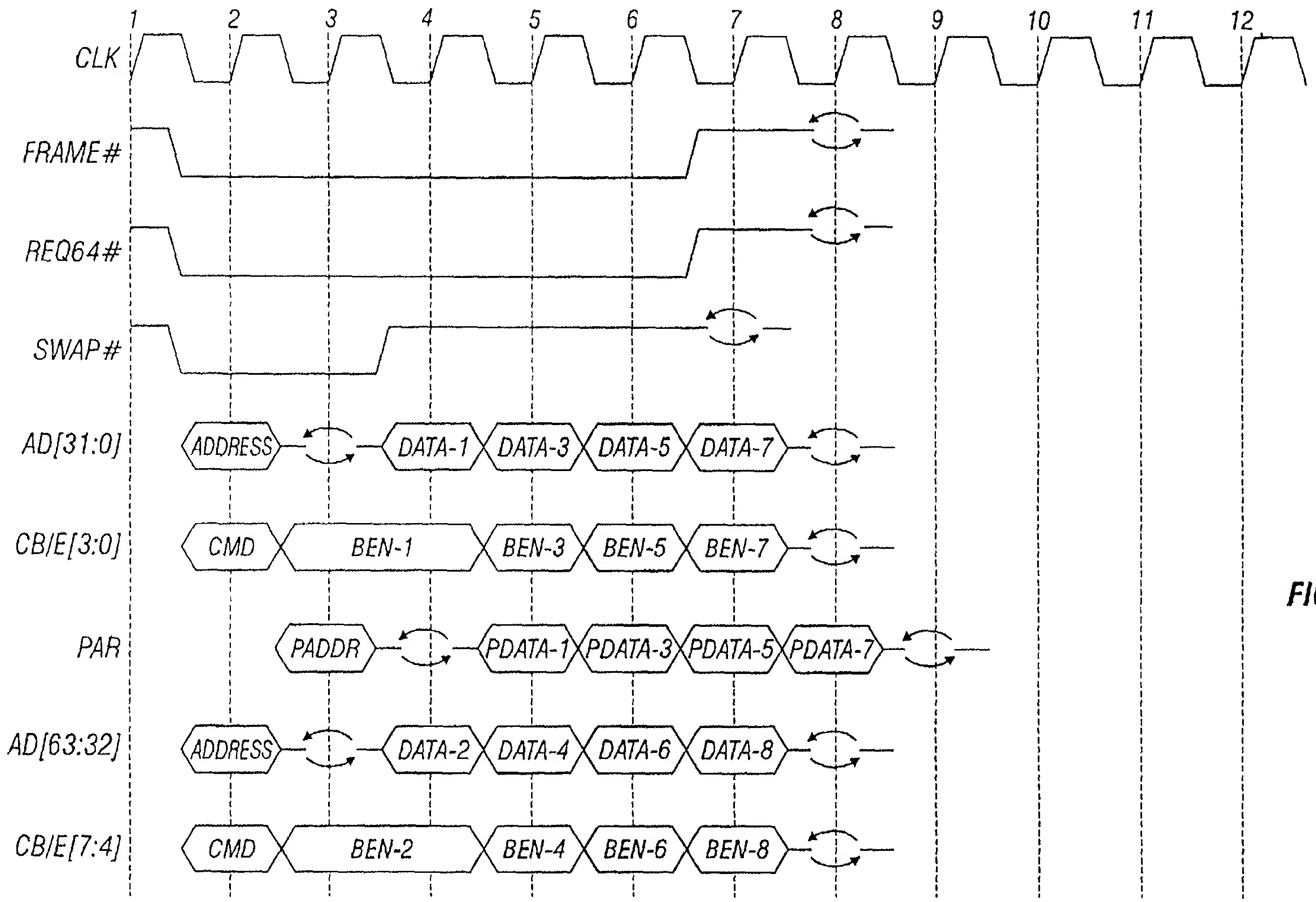

FIG. 15A

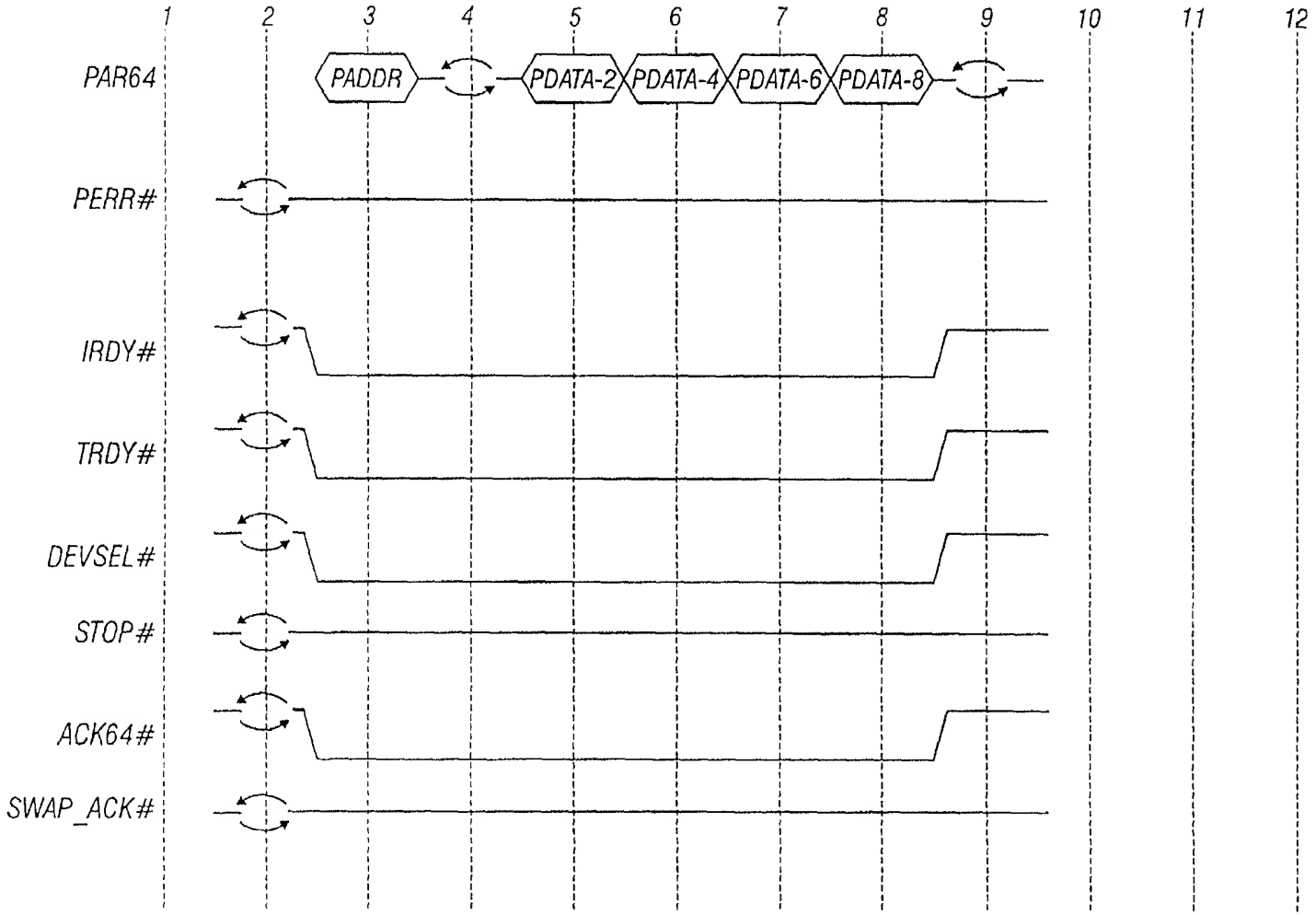
1
2
3
4
5
6
7
8
9
10
11
12
PAR64
PADDR
PDATA-2
PDATA-4
PDATA-6
PDATA-8
PERR#
IRDY#
TRDY#
DEVSEL#
STOP#
ACK64#
SWAP_ACK#

FIG. 15B

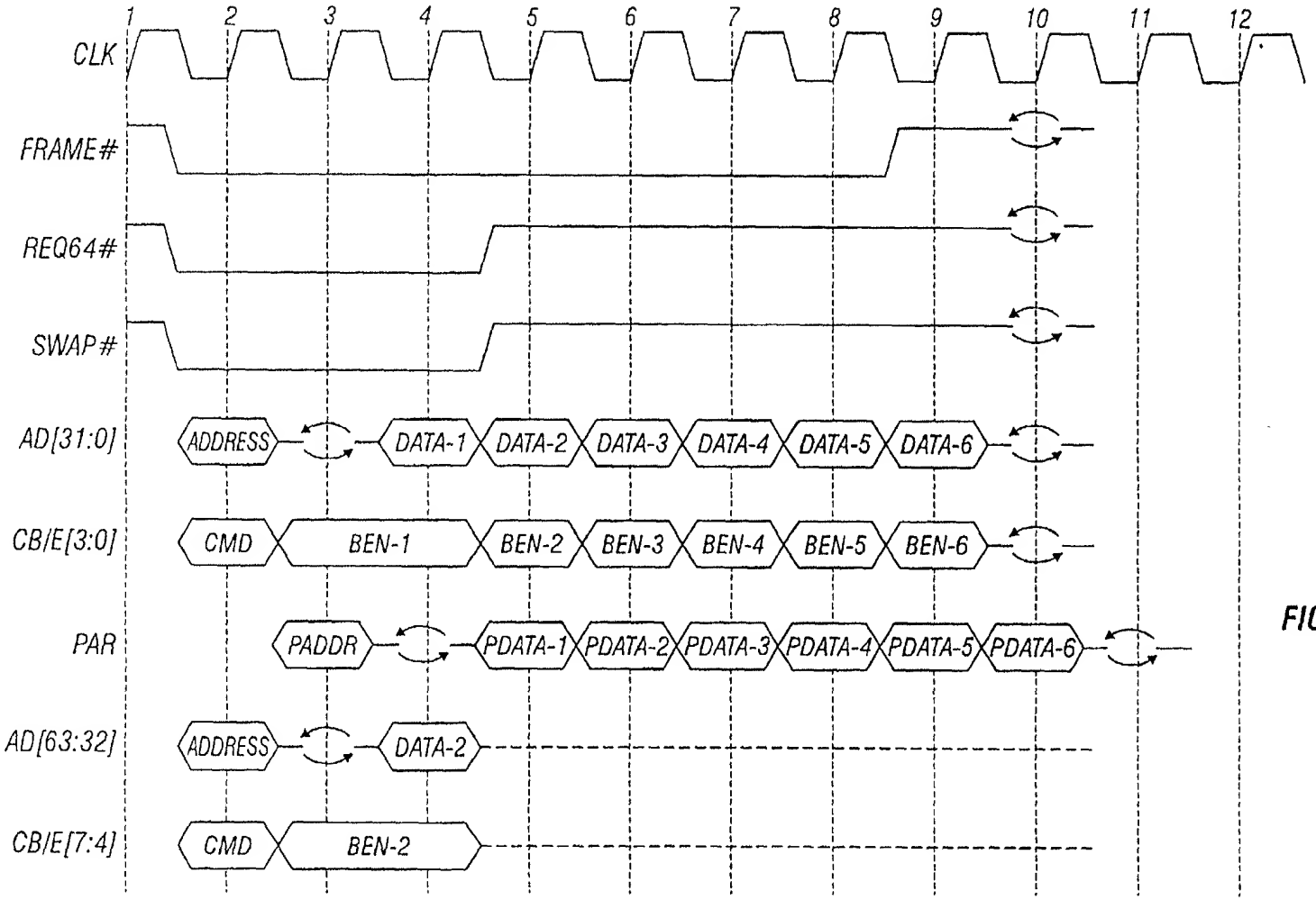
1
2
3
4
5
6
7
8
9
10
11
12
CLK
FRAME#
REQ64#
SWAP#
AD[31:0]
ADDRESS
DATA-1
DATA-2
DATA-3
DATA-4
DATA-5
DATA-6
CB/E[3:0]
CMD
BEN-1
BEN-2
BEN-3
BEN-4
BEN-5
BEN-6
PAR
PADDR
PDATA-1
PDATA-2
PDATA-3
PDATA-4
PDATA-5
PDATA-6
AD[63:32]
ADDRESS
DATA-2
CB/E[7:4]
CMD
BEN-2

FIG. 16A

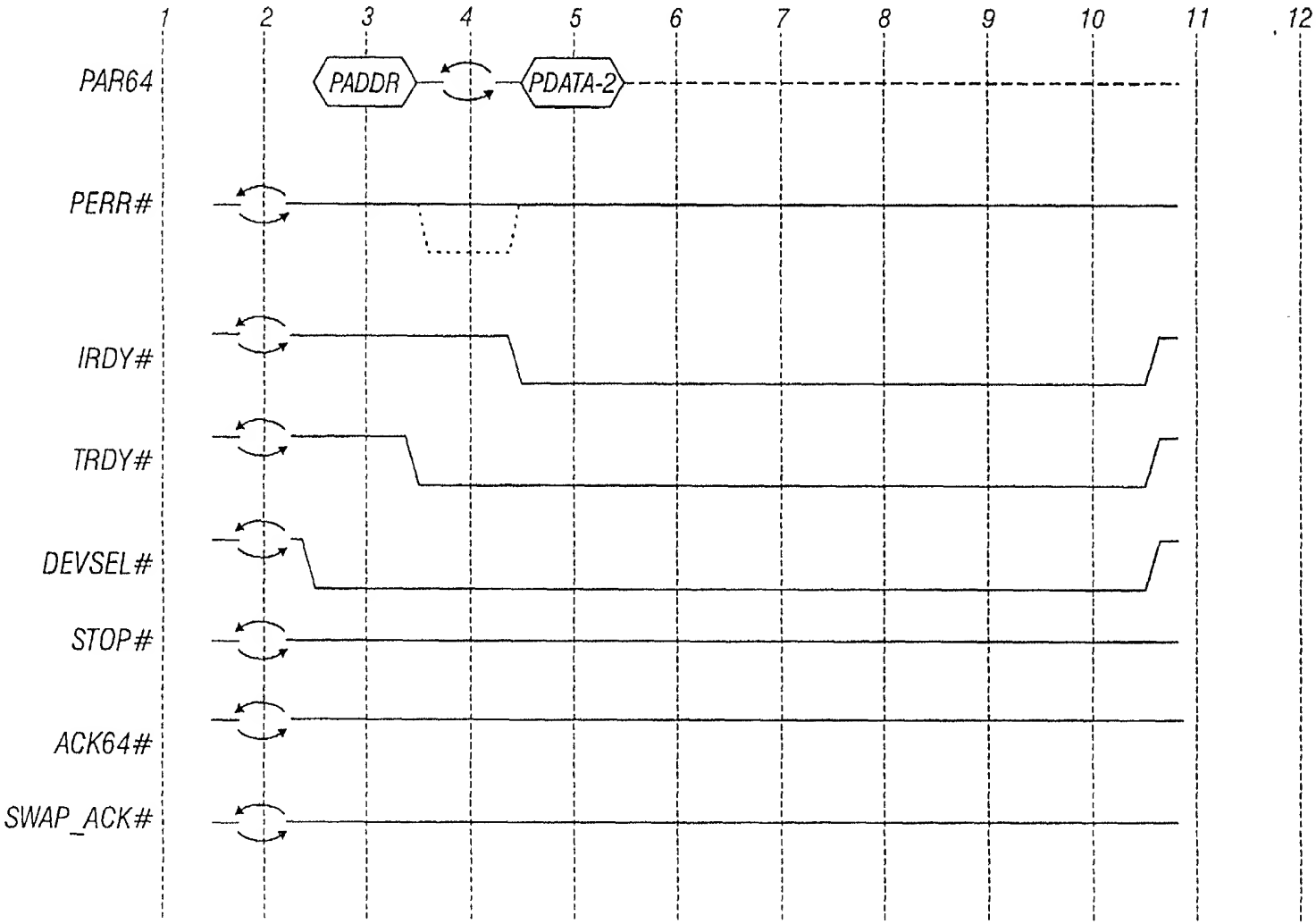
1
2
3
4
5
6
7
8
9
10
11
12
PAR64
PADDR
PDATA-2
PERR#
IRDY#
TRDY#
DEVSEL#
STOP#
ACK64#
SWAP_ACK#

FIG. 16B

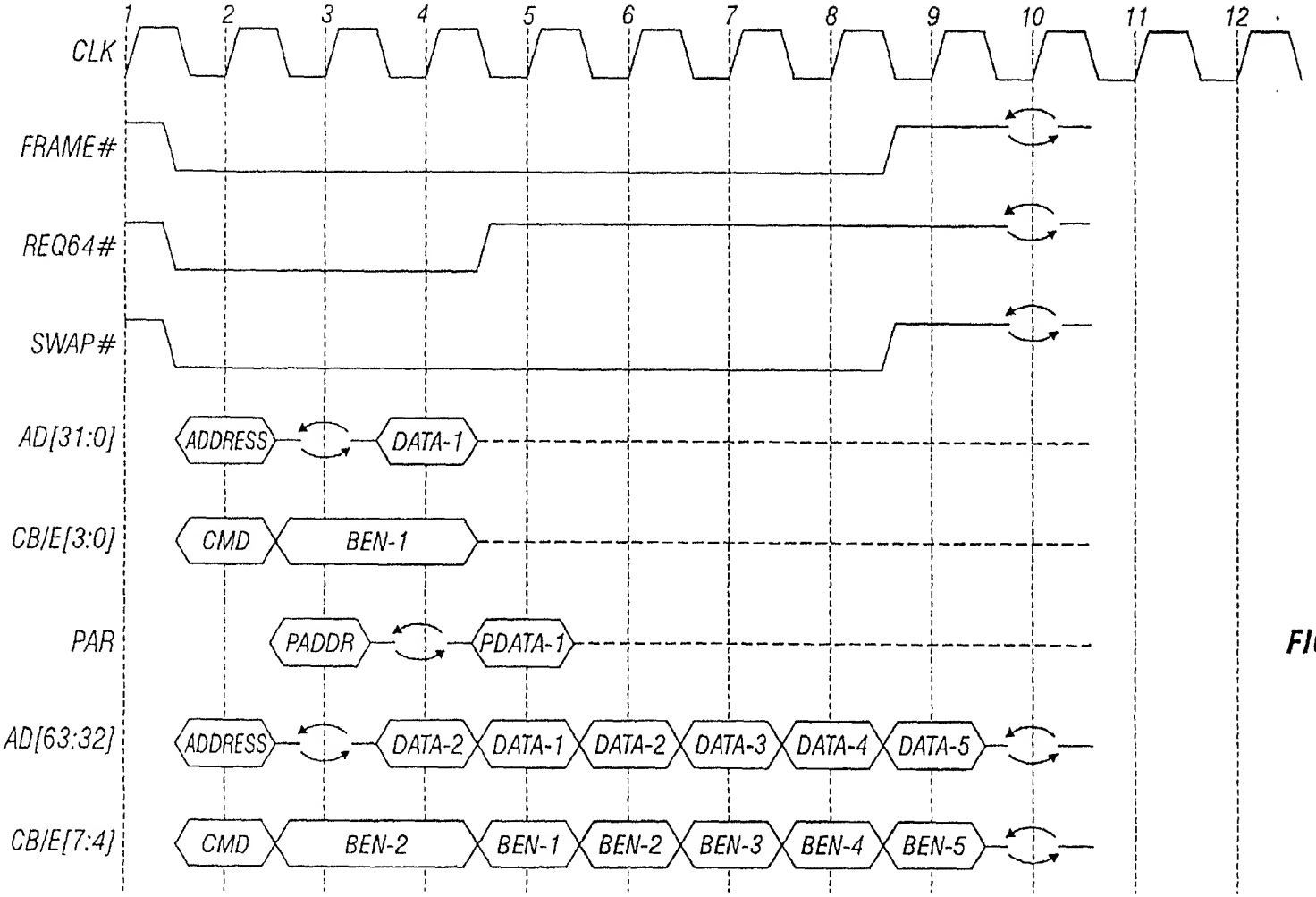
1
2
3
4
5
6
7
8
9
10
11
12
CLK
FRAME#
REQ64#
SWAP#
AD[31:0]
ADDRESS
DATA-1
CB/E[3:0]
CMD
BEN-1
PAR
PADDR
PDATA-1
AD[63:32]
ADDRESS
DATA-2
DATA-1
DATA-2
DATA-3
DATA-4
DATA-5
CB/E[7:4]
CMD
BEN-2
BEN-1
BEN-2
BEN-3
BEN-4
BEN-5

FIG. 17A

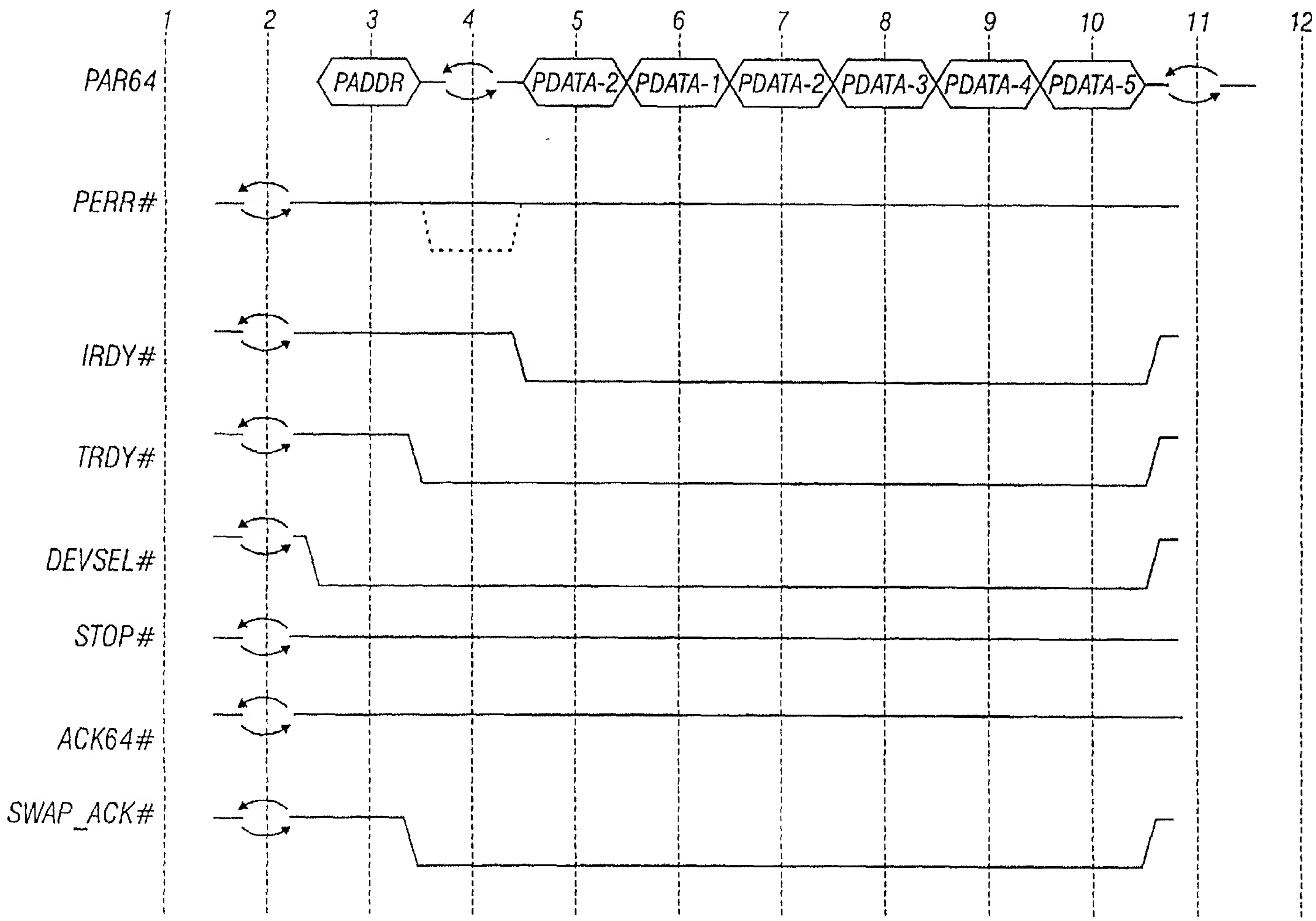

FIG. 17B

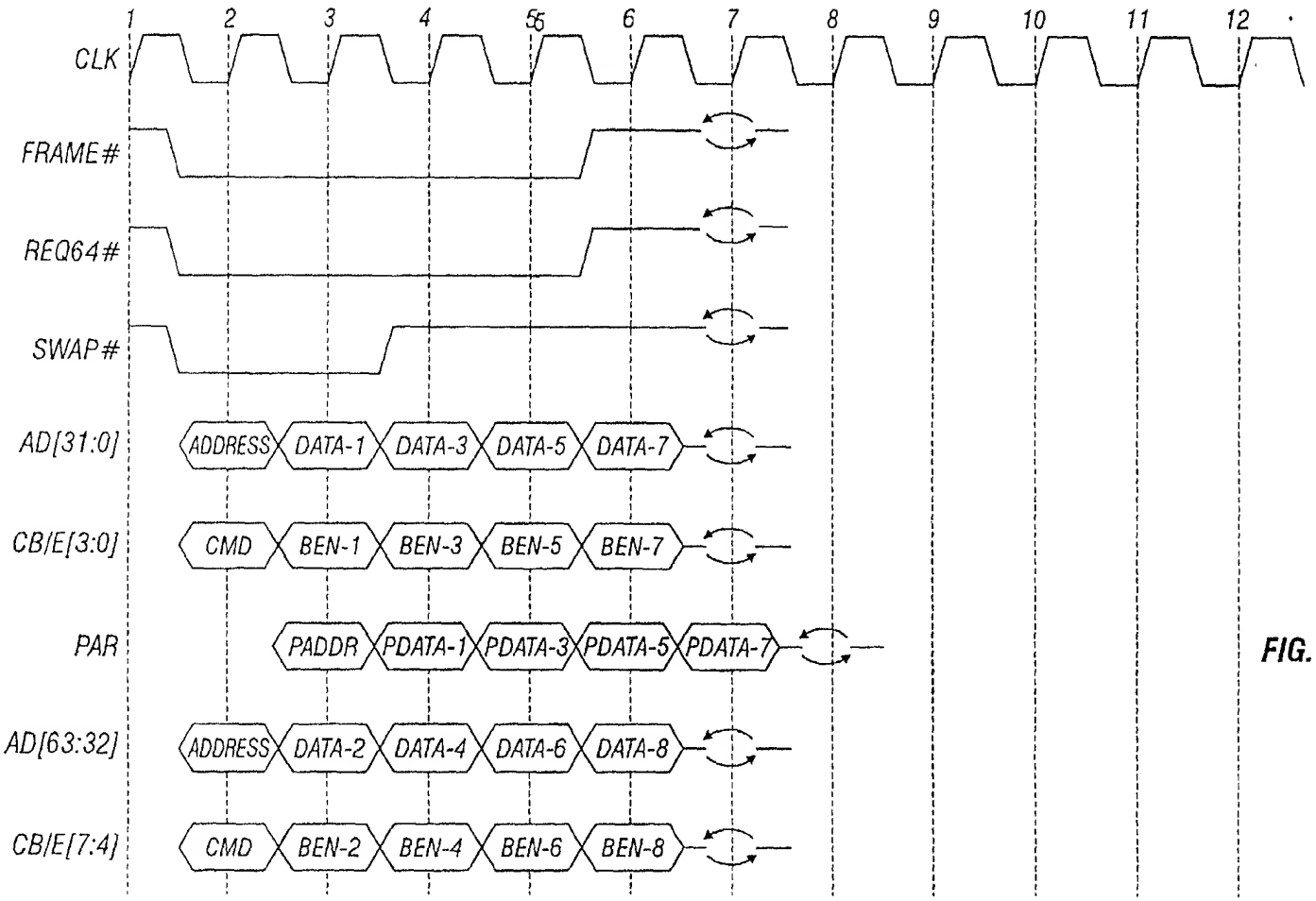
1
2
3
4
5
6
7
8
9
10
11
12
CLK
FRAME#
REQ64#
SWAP#
AD[31:0]
ADDRESS
DATA-1
DATA-3
DATA-5
DATA-7
CB/E[3:0]
CMD
BEN-1
BEN-3
BEN-5
BEN-7
PAR
PADDR
PDATA-1
PDATA-3
PDATA-5
PDATA-7
AD[63:32]
ADDRESS
DATA-2
DATA-4
DATA-6
DATA-8
CB/E[7:4]
CMD
BEN-2
BEN-4
BEN-6
BEN-8

FIG. 18A

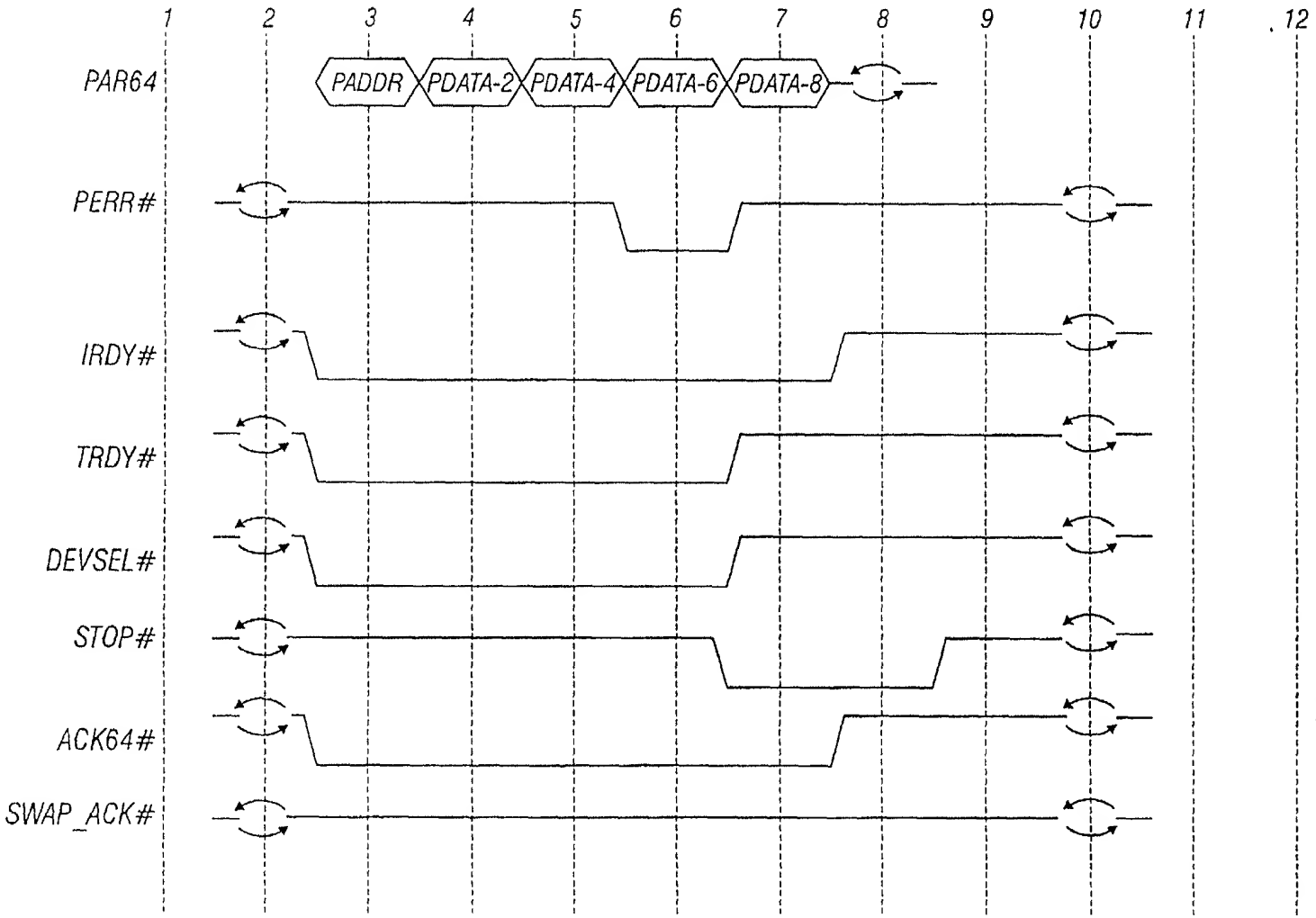
1
2
3
4
5
6
7
8
9
10
11
12
PAR64
PADDR
PDATA-2
PDATA-4
PDATA-6
PDATA-8
PERR#
IRDY#
TRDY#
DEVSEL#
STOP#
ACK64#
SWAP_ACK#

FIG. 18B

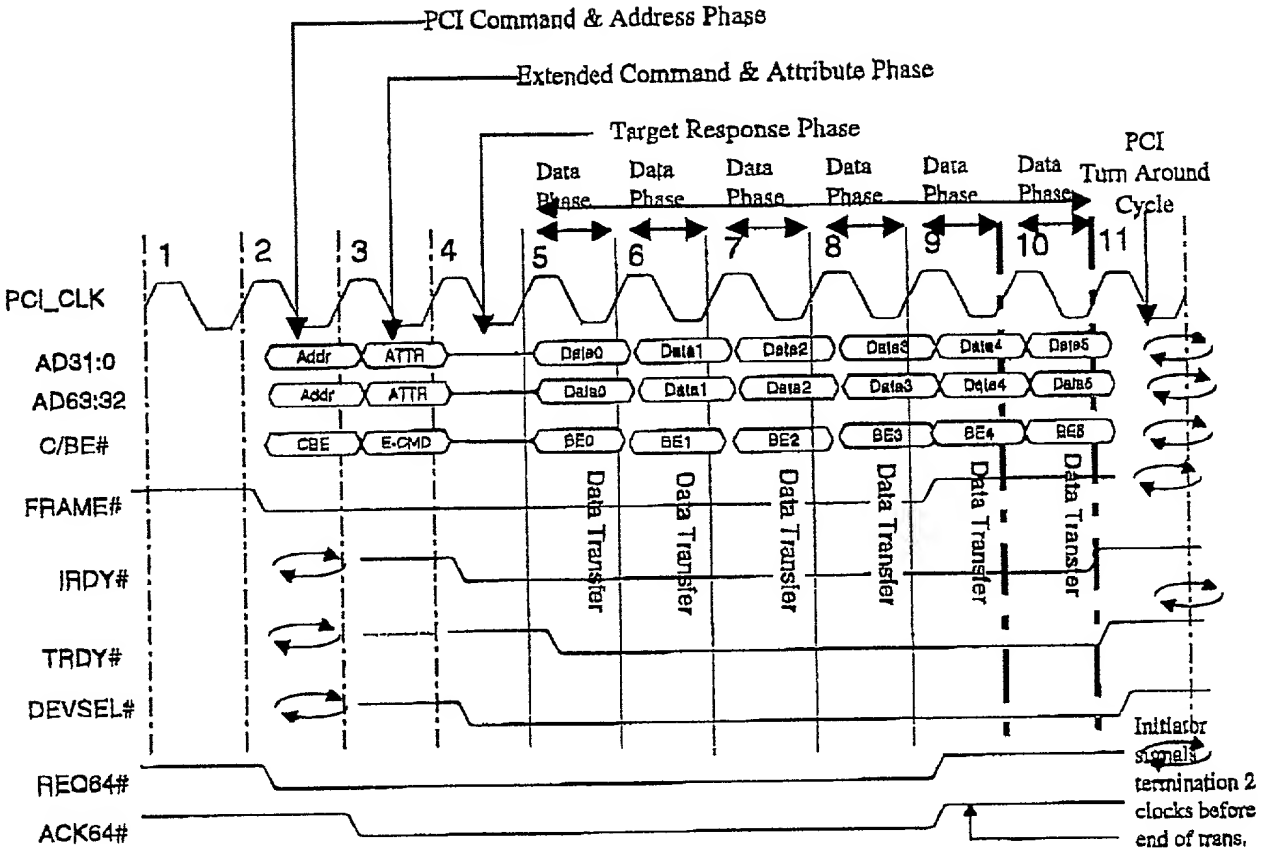
PCI Command & Address Phase
Extended Command & Attribute Phase
Target Response Phase
Data Phase
Data Phase
Data Phase
Data Phase
Data Phase
Data Phase
PCI Turn Around Cycle
1
2
3
4
5
6
7
8
9
10
11
PCI_CLK
AD31:0
AD63:32
C/BE#
FRAME#
IRDY#
TRDY#
DEVSEL#
REQ64#
ACK64#
Addr
ATTR
CBE
E-CMD
Data0
Data1
Data2
Data3
Data4
Data5
BE0
BE1
BE2
BE3
BE4
BE5
Data Transfer
Initiator signals termination 2 clocks before end of trans.

FIG. 19

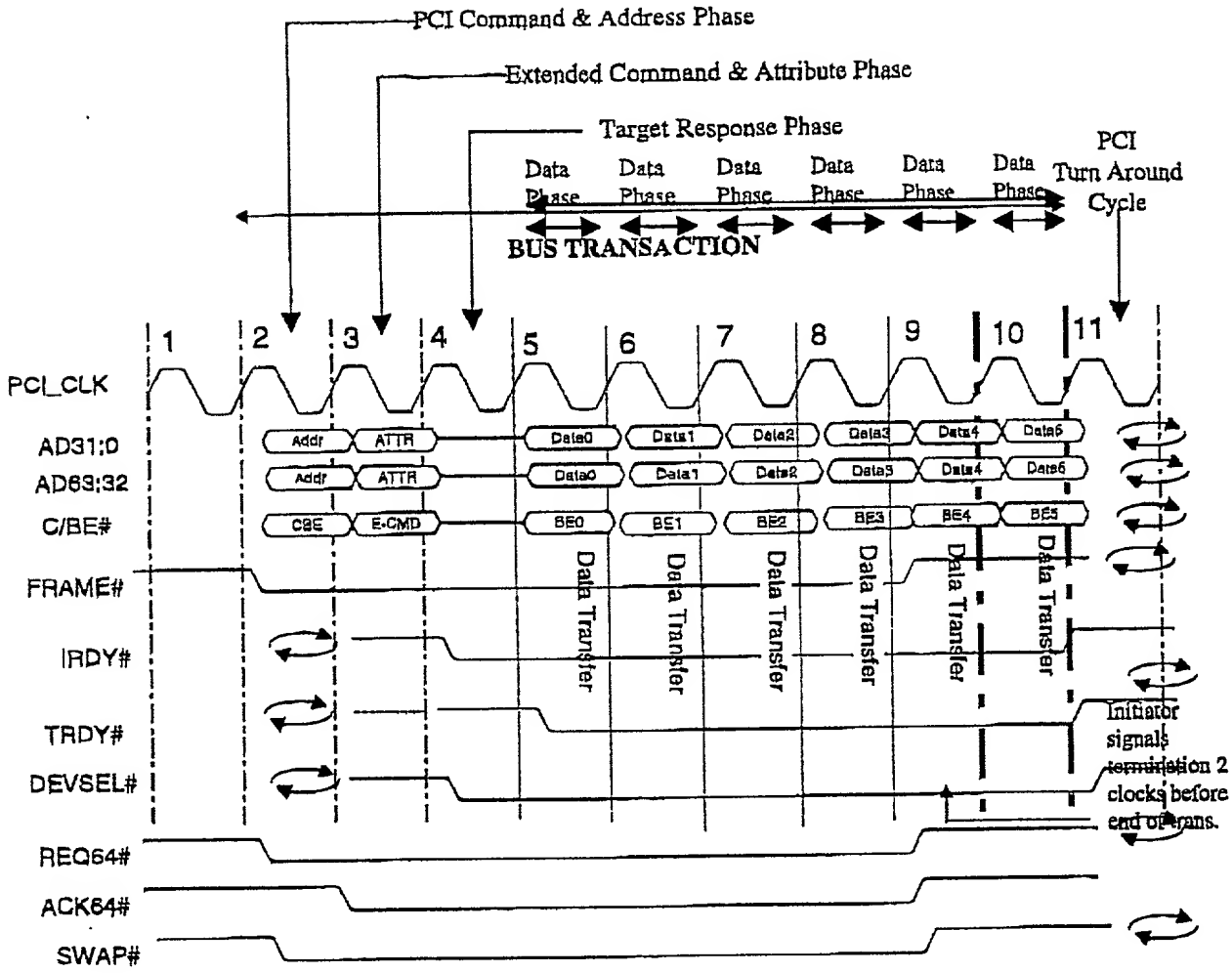
PCI Command & Address Phase
Extended Command & Attribute Phase
Target Response Phase
Data Phase
Data Phase
Data Phase
Data Phase
Data Phase
Data Phase
PCI Turn Around Cycle
BUS TRANSACTION
1
2
3
4
5
6
7
8
9
10
11
PCI_CLK
AD31:0
AD63:32
C/BE#
FRAME#
IRDY#
TRDY#
DEVSEL#
REQ64#
ACK64#
SWAP#
Addr
ATTR
C8E
E-CMD
Data0
Data1
Data2
Data3
Data4
Data5
Data6
BE0
BE1
BE2
BE3
BE4
BE5
Data Transfer
Initiator signals termination 2 clocks before end of trans.

FIG. 20